Measurements in digital component television studios

625–line systems at the 4:2:2 and 4:4:4 levels
using parallel and serial interfaces (SDI)

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CONTENTS

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Introduction

This EBU technical document is a guide to the assessment of technical performance in television studios which are designed entirely on the basis of digital component technology, or which incorporate such technology for use in conjunction with analogue systems.

Interfacing is an important consideration in such installations, and in view of the fact that in many cases signal characteristics can only be measured at the input and outputs of equipment, measurements on parallel and serial interfaces carrying 625–line digital component video signals at the 4:2:2 level are a prominent feature of this document. Measurements on ancillary data signals including, notably, audio signals conforming to the AES/EBU digital audio standard, are also dealt with in some detail. In contrast, the performance of individual types of equipment found in a modern digital component studio environment – digital video effects systems, mixers, etc. – is not considered in any depth, except to the extent that inadequate performance (or constraints such as signal delays imposed by the type of processing involved) may have a wider impact on the overall performance through a digital production chain.

The general principles of performance measurement set out in this document are also applicable to the 4:4:4 configuration of digital component television signals. Whereas, at the 4:2:2 level, a single serial or parallel interface carries a wide–band luminance signal and two colour–difference signals of lower bandwidth, at the 4:4:4 level two interfaces are used together to carry a total of four wide–band signals. These may be red, green and blue primary signals, or luminance and two colour–difference signals; in either case, the fourth channel can be used for an additional wideband signal such as an associated key signal.

The serial digital interface (SDI) can also be used to convey other forms of television signal such as 525–line 4:2:2 digital component video or digital PAL sampled at four times the colour subcarrier frequency. While much of the discussion in this document is relevant also to these signal formats, no specific reference is made to the corresponding parameter values.

The document is for the use of engineers who need to carry out measurements on digital video and audio systems. Such measurements may be necessary for many reasons: planning and installation, acceptance testing, maintenance and the checking of signals during programme production or play–out.

A number of different technologies are involved and it is not possible to treat each one in isolation. The serial digital interface (SDI), combining 4:2:2 component video, AES/EBU audio, time code, signalling etc. into a single data–stream at 270 Mbit/s is the most complex of a range of digital signal configurations found in the television production environment. The correct functioning of these systems requires that consideration be given to certain aspects of the analogue video and audio signals, the waveform parameters and logic levels of the digital interface signal itself, and a number of peripheral aspects such as conversion between the analogue and digital domains, PAL encoding, etc.

The formal characteristics of the signals and interfaces involved in digital television production are set out in a number of standards documents, which are reviewed in *Chapter 1*. These standards define the conversion of a video signal from its analogue form (PAL colour, *RGB* primaries or analogue components), and the characteristics of the corresponding digital signals, which must be adhered to if compatibility is to be assured. These signal standards and the parallel and serial interface formats represent the main emphasis of digital television technology today and, despite its relative complexity and sensitivity to external influences, the 270 Mbit/s serial digital interface is supported by all modern digital television equipment.

Chapter 2 is concerned with measurements in the analogue domain, and the relationships between analogue signals and the digital representations carried through the parallel interface and the SDI. Although much of the content of this document is concerned with digital interface performance, it should not be overlooked that the overall performance of the programme chain will be less than optimal if, for example, an analogue source signal does not confom to the relevant specifications, an analogue–to–digital converter is mis–aligned, or the analogue display system is mal–functioning.

Chapter 3 is concerned with the data conveyed through a digital production system: validity of the transmitted data, timing, etc., whilst *Chapter 4* gives details of a range of measurement procedures covering the physical characteristics of both parallel and serial interfaces: waveforms, signal levels, jitter, for example.

Chapter 5 is concerned more generally with the way in which the digital component interfaces fit into the working environment of the modern production area.

Digital video interfaces employ very sophisticated data transmission techniques and require the use of specialized measurement instruments. *Chapter 6* discusses the characteristics and features of suitable test instruments and test signals.

The document includes a *Reference data and Standards* section giving all the principal technical parameters of the interfaces discussed in the document and a list of relevant standards documents.

Finally, a number of *Appendices* give further background explanations on several important measurement concepts relating to the serial digital interface and test instruments for digital video signals.

Important notes

1. In this document, the more common signal nomenclature $Y/C_B/C_R$ is used to designate analogue component signals, instead of the E'_Y, E'_{CB}, E'_{CR} nomenclature specified in the relevant standards, although in principle $Y/C_B/C_R$ refers to the digital representations of analogue component signals.
2. The PAL system has been used in this document to represent composite analogue signals. Statements concerning composite PAL are basically applicable also to SECAM systems.
3. Digital component television systems covered by this document may use 8–bit or 10–bit representations of signal levels. Where information relates specifically to 10–bit representation, the values are enclosed in angle brackets, thus: <...>.
4. Descriptions of digital video systems require the use of several different number representations.

   All values in hexadecimal notation are indicated in the form: NN_{hex}.

   Decimal numbers are shown with the subscript NN_{dec} only where necessary to avoid ambiguity.
5. The text includes cross–references to three independent sets of reference information:

References to	*Form of cross–reference*	*Link to*
Reference data extracted from the relevant standards documents	*Ref. n*	*Reference data and Standards* section (coloured pages)
Titles of formal standards, specifications and other documents defining interfaces, test methods or related aspects	[S.n]	
Sources giving general background information	[n]	*Bibliography* (back of book)

Chapter 1

Presentation of digital component interfaces

This Chapter gives a general presentation of the digital component video standards covering television signal formats, their data representations and physical interface configurations.

1.1. The 4:2:2 digital video format

ITU–R Recommendation BT.601 [S.1] defines the signal sampling parameters used in the conversion of 625–line video signals from the analogue to the digital domain. It also defines the characteristics of the anti–aliasing filters needed at the input of the conversion process in order to minimize under–sampling artefacts.

1.1.1. Sampling

a) Sampling frequency

The designation “4:2:2” signifies the ratio of the sampling frequencies for the luminance and chrominance components of the analogue signal. ITU–R Recommendation BT.601 specifies a sampling frequency of 13.5 MHz for the luminance component, Y, and 6.75 MHz for each of the chrominance signals, C_B and C_R.

The sampling frequencies are integer multiples of the line frequency, F_h, and ITU–R Recommendation BT.601 specifies the same sampling scheme for both the 625 and 525–line standards (625 lines: 864 x F_h = 13.5 MHz; 525 lines: 858 x F_h = 13.5 MHz).

The choice of sampling frequency defines the maximum signal bandwidth. According to the theories of Shannon and Nyquist, the sampling frequency should be at least twice the maximum signal frequency if aliasing effects are to be avoided. This means that the maximum theoretical signal bandwidths are 6.75 MHz for the luminance and 3.375 MHz for each chrominance signal.

ITU–R Recommendation BT.601 [S.1] gives tolerances for the input filter bandwidth, resulting in a restriction of the bandwidths to less than these theoretical values. The luminance channel specification requires the attenuation to be less than 0.1 dB at 5.75 MHz, greater than 12 dB at 6.75 MHz and greater than 40 dB at frequencies in excess of 8 MHz. For the chrominance channels the attenuation should be less than 0.1 dB at 2.75 MHz, more than 6 dB at 3.375 MHz and more than 40 dB at frequencies in excess of 4 MHz.

To accommodate wide–screen applications, ITU–R Recommendation BT.601 has been extended to include a sampling frequency of 18 MHz (4/3 x 13.5 = 18). The EBU does not support the use of two different sampling frequencies, and has stated its preference for a single sampling frequency of 13.5 MHz [S.2]. This is for operational convenience, and because the bandwidth restrictions of existing and potential delivery systems prevent the additional horizontal resolution, associated with the higher sampling frequency, from being seen by viewers.

b) Sampling structure

ITU–R Recommendation BT.601 describes the orthogonal sampling structure of the signal and EBU document Tech. 3267 [S.3] sets out the manner in which the sample values are multiplexed into the data–stream. The most important features of the arrangement are shown in *Ref. 1* and *Ref. 2* in the *Reference data and Standards* section.

There are 720 luminance samples (Y) and 360 samples for each chrominance signal (C_B, C_R), making a total of 1440 samples per active line. The first three samples of the active line are numbered $C_B/Y/C_R$ = 0/0/0 and the last four samples have numbers $C_B/Y/C_R$ = 359/718/719. The first sample after blanking is always a C_B value and the last sample is always a Y value. (This is the same in both 525– and 625–line systems.)

The first sample in the active video, sample C_B–0, occurs 132 sampling periods after the leading edge of the analogue line synchronization pulse. The digital blanking period is 10.7 µs, and the analogue blanking is 12 µs. The digital active line is therefore 1.3 µs longer than the analogue active line (*Ref. 1)*.

1.1.2. Quantization of video signals

The quantization of signals in the digital domain is governed by five considerations:

– maximum number of values represented by the quantizing scale;
– nominal range of levels (i.e. the range of values covered by the quantizing levels);
– level headroom;
– number of bits per sample;
– excluded codes, reserved for synchronization purposes.

The maximum number of values, specified in ITU–R Recommendation BT.601, is 256 <1024>[1], for both the luminance and the chrominance components.

Ref. 7 and *Ref. 8* show the digital values of the luminance and chrominance components, with the corresponding values in binary, decimal and hexadecimal notation. These diagrams clearly show the values which are forbidden, as discussed in *Sections 1.1.2.a)* and *b)* below (e.g. 00.0_{hex} to $00.C_{hex}$ and $FF.0_{hex}$ to $FF.C_{hex}$ in 10–bit luminance coding).

a) Luminance (Ref. 7)

The active luminance signal, Y, uses 220 <877> levels only. The remaining 36 <147> levels above and below the signal range are reserved for headroom and synchronization.

The analogue signal range for the Y signal is from 0 mV to 700 mV. The quantization is linear, and each quantizing step corresponds to an analogue level difference of about 3.2 mV <0.8 mV>.

Quantizing levels 1 to 15 <4 to 63> and 236 to 254 <941 to 1019> are reserved for the lower and upper headrooms, respectively.

Synchronization codes are reserved for timing reference signals (TRS). The TRS preambles are:

FF_{hex}	00_{hex}	00_{hex}	for 8–bit systems
$FF.C_{hex}$	00.0_{hex}	00.0_{hex}	for 10–bit systems.

b) chrominance (Ref. 8)

The nominal range of values for each chrominance signal extends from 16 to 240 <64 to 960>, allowing 225 <897> values to be used. The chrominance signals lie symmetrically around level 128, corresponding to 0 mV. The quantization step is about 3.1 mV (0.87 mV).

Levels 1 to 15 <4 to 63> and 241 to 254 <961 to 1019> are reserved for the lower and upper headrooms.

1.1.3. Coding

The first systems for digital video used a coding scheme with 8 bits per sample. The need for better amplitude resolution (initially to preserve the additional bits generated during processing, but also to improve the signal–to–noise ratio) led to the introduction of 10–bit versions of the sampling and interface standards.

1. Where information relates specifically to 10–bit representation, the values are enclosed in angle brackets, thus: <...>.

ITU–R Recommendation 601 describes 8–bit and 10–bit coding. To facilitate interpretation of sample values, 10–bit values are considered as 8–bit integer values with two additional fractional bits.

For example:

	bit pattern	*decimal value*	*hex value*
8–bit	1001 0001	145_{dec}	91_{hex}
10–bit	1001 0001.01	145.25_{dec}	91.4_{hex}

The fractional part of the 10–bit word can have one of four values:

00	=	$.00_{dec}$	=	$.0_{hex}$
01	=	$.25_{dec}$	=	$.4_{hex}$
10	=	$.50_{dec}$	=	$.8_{hex}$
11	=	$.75_{dec}$	=	$.C_{hex}$

If no fractional part is present, then the two bits are interpreted as zero.

1.1.4. Timing reference signals (TRS – EAV, SAV)

Each line of the digital frame is identified by its timing reference signal, comprising the three–word timing reference sequence and the fourth word which marks either the *end of active video* (EAV) or *start of active video* (SAV). The structure of the TRS is specified in EBU document Tech. 3267 [S.3] and the principal features are shown in *Ref. 6.*

The start of digital blanking is marked by the insertion of the EAV code in sample positions 360/720/360/721, and the end of digital blanking is marked by the SAV code in sample positions 431/862/431/863 *(Ref. 2).*

1.1.5. Ancillary data

a) General

In addition to the digital video signal, the interfaces have capacity for ancillary data signals. All data in the period from the end of active video (EAV) to the start of active video (SAV), excluding the EAV and SAV timing reference signals (TRS), is referred to as “horizontal ancillary data (HANC)”. Data in the active part of the lines in the vertical blanking interval is referred to as “vertical ancillary data (VANC)”. These ancillary data areas may carry digital audio channels, digital time–code (DTC), or similar information.

SMPTE Standard 291M [S.9] specifies that ancillary data in both the VANC and HANC should use a 10–bit structure.

The structure of the ancillary data message is shown in *Ref. 9.*

Ancillary data packets have a preamble called the ancillary data flag (ADF) consisting of three words with the following values:

$$00.X_{hex}, \quad FF.X_{hex}, \quad FF.X_{hex}.$$

The three words following the ADF comprise

either: a data identification (DID), a data block number (DBN) and data count (DC),

or: a data identification (DID), a secondary data identification (SDID) and a data count (DC).

Words in the horizontal and vertical blanking intervals which are neither timing reference signals (TRS) nor active ancillary data should be replaced with the following values:

$$80.0_{hex}, \quad 10.0_{hex}, \quad 80.0_{hex}, \quad 10.0_{hex}, \quad \text{etc.} \quad (C_B/Y/C_R/Y/...).$$

Some of the lines in the vertical–blanking interval are reserved for purposes other than ancillary data:

lines 20, 333:	self–test purposes;
lines 6, 7, 8, 319, 320, 321:	must not contain ancillary data, to avoid problems during video switching (see *Ref. 14*);
lines 11, 324:	should not be used for audio or extended data.

b) Insertion of AES/EBU digital audio as ancillary data

Up to 16 AES/EBU digital audio signals, each conveying one pair of audio channels with 20–bit (optionally, 24–bit) coding, can be inserted as ancillary data.

The audio data is sampled continuously but when it is carried in the SDI the audio data–stream is inserted only during the horizontal and vertical blanking intervals. This implies the provision of a buffer memory to permit continuous input and output of audio data–streams.

The full specifications of AES/EBU digital audio signals are given in the relevant standards documents: EBU document Tech. 3250 [S.26][S.27][S.28] and AES3 [S.29]. The audio frame structure is shown in *Ref. 10.*

Specifications for the insertion of AES/EBU audio into the serial digital interface are given in SMPTE Standard 272M [S.32].

The insertion of audio data in the ancillary data packets of the SDI is shown in *Ref. 11*. The 20–bit audio sample word plus the three following bits (validity bit, user bit and audio channel status) of a particular audio channel (i.e. the left or right channel of a particular audio channel pair) are mapped into three consecutive words of an SDI ancillary data packet, labelled as an "audio" data packet. The four auxiliary data bits which precede the 20–bit sample data in the audio sub–frame are mapped into data words in an ancillary data packet of the SDI, labelled as an "extended" data packet. Each extended data packet word carries auxiliary data bits from two audio sub–frames.

Measurement procedures for digital audio signals are set out in AES 11 [S.41] and AES 17 [S.42].

c) Insertion of digital time–code in the ancillary data

A specification for digital time–code (DTC) is under study within the EBU and the SMPTE.

d) Error detection and handling (EDH)

SMPTE Recommended Practice RP 165 [S.39] defines an error detection and handling (EDH) system based on the use of appropriate forms of check–word (e.g. cyclic redundancy check – CRC) and status flags.

The CRC code used is the standard 16–bit CRC–CCITT polynomial code, having the polynomial function $x^{16} \oplus x^{12} \oplus x^5 \oplus 1$, where $\oplus$ is the exclusive–OR function.

The CRC is applied over the complete digital chain. The proposal foresees the continuous generation of three CRCs, calculated over three different areas of the data–stream:

– the active picture samples;

– the full field;

– the ancillary data.

The check words and the status flags are combined in an "error status packet" which is inserted as ancillary data in lines 5 (words Y850 – Y861 <Y1138 – Y1149>) and 318 of the next–following field. The full–field check words are calculated on the samples of all the lines except those containing the error status packet and the two immediately–following lines (vertical–interval switching area).

At the SDI receiver, the same check–words are calculated from the received data–stream, using the same techniques as in the transmitting equipment, and they are compared with those extracted from the error status packet. The presence of an error determines the generation of a flag indicating the detection of an error. Three error flags are provided (one corresponding to each of the three CRCs listed above) and they refer to the status of the *previous* field.

1.2. Other digital component signal formats

EBU document Tech. 3268 [S.4] defines an additional format with 4:4:4 sampling for use in equipment requiring high–quality signal processing and for chroma–key capability. As noted in the *Introduction*, a 4:4:4 interface comprises two 4:2:2 interfaces operating in parallel and in many respects the guidance given in the present document is relevant also to measurements on 4:4:4 interfaces.

There exist also some other designations which include a fourth parameter, such as 4:2:2:4 or 4:4:4:4, in which the last digit gives the ratio of the sampling frequency for the key system (13.5 MHz if the digit is 4). In the last case two interfaces are needed because there is twice as much data, compared to a 4:2:2 system.

Sub–sets of the main 4:2:2 format include the 4:2:1, 4:2:0.5, 4:2:0 and 4:1:1 formats.

The serial digital interface can also be used to convey digital PAL signals sampled at four times the colour subcarrier frequency ($4f_{sc}$ = 17.734475 MHz). The digital PAL signal is specified in EBU document Tech. 3280

[S.18]. It uses 8–bit quantizing carried in 10–bit data words to achieve compatibility with the SDI data format and the data rate of the serial digital PAL signal is 177.34 Mbit/s.

1.3. Other standards to be considered

Although this document is concerned very largely with measurements on standard digital component video interfaces, it is important to be aware of the possible effects of signal processing in equipment which is fitted with these interfaces. Digital video recording systems and equipment using bit–rate reduction technologies may cause unexpected difficulties when making measurements on interface signals.

1.3.1. Digital video recording standards D1 to D6

Although the digital VTR standards share the common serial digital interface, there are variations in their internal signal processing. The variations are summarized in *Table 1*.

Table 1 – Principal characteristics of digital video recording formats.

Format	Signal system	Video data bits	BRR	VBI lines recorded	Sampling frequency (MHz)	Standards	Notes
D1	Component	8	No	11–22 324–335	13.5/6.75/6.75	IEC 1016 [S.43] ITU–R BT.657 [S.44]	6, 7
D2	Composite	8	No	7/8/9/10–22 320/321/322/323–335	17.72 (PAL)	IEC 1079 [S.46] SMPTE 244 M [S.8]	1
D3	Composite	8	No	7/8–22 320/321–335	17.72 (PAL)	SMPTE 244 M [S.8]	1
DCT	Component	8	2:1	11–22 324–335	13.5/6.75/6.75		2, 7
D5	Component	10	No	8–22 312–335	13.5/6.75/6.75 18/9/9		3, 7
Digital Betacam	Component	8/10	2:1	8–22 312–335	13.5/6.75/6.75		4, 7
D6	Component	8	No	21–44 , 646–669 38–40 , 601–602	72/36/36 74.25/37.125/37.125	EU 95 SMPTE 240 M [S.11] SMPTE 260 M [S.12] ITU–R BT.709 [S.16]	5

Notes:
1 141 Mbit/s for PAL; selection of recorded VBI lines depends on PAL 8–field sequence.
2 10–bit video data words are rounded to 8–bits prior to recording.
3 360 Mbit/s for 8–bit resolution.
4 Analogue inputs use 8–bit data only.
5 HDTV recorder (1250/50 for Eureka 95 project, 1125/60 for US).
6 Signal format defined in ITU–R Recommendation BT.601 [S.1].
7 Interface defined in ITU–R Recommendation BT.656 [S.5].

1.3.2. Equipment using bit–rate reduction

The picture quality obtained in systems using bit–rate reduction (BRR) depends on the structure of the active picture and the vertical blanking interval. The use of BRR can destroy the insertion test signals (ITS) and data signals in the vertical blanking interval, and some special test signals carried in the active picture area. Standards documents defining systems which use BRR include the following:

– ITU–R Recommendation 721 [S.13], which describes the transmission of digital component television signals at bit–rates close to 140 Mbit/s for contribution purposes;

– ITU–R Recommendation BT.723 [S.14] and European Telecommunication Standard ETS 300 174 [S.15], which give the bit–rated reduced (34–45 Mbit/s) transmission format for contribution–quality signals corresponding to the 4:2:2 SDI interface;

– the MPEG–2 standards for bit–rate reduced video signals in the 1.2 to 3 Mbit/s, 5 to 10 Mbit/s, 7 to 15 Mbit/s and 20 to 40 Mbit/s hierarchies; although these signals cannot be synchronized to the SDI signal it is possible to use the 4:2:2 interface as a transport stream (see *Section 1.3.3.*).

1.3.3. Data–rate and format conversion

There are several systems in use for the transmission of component–coded television signals which, though the use of compression techniques, use data formats and data–rates different to those of the SDI. The SDI can carry compressed signals in a variety of formats provided that the basic data structure (TRS) of the SDI signal is maintained.

Measurement procedures for such signals are under discussion.

a) ATM interfaces

The asynchronous transfer mode (ATM) is used as a transport medium for video, audio and data in a small number of applications, but its use in a broadcast studio environment has not been examined in detail.

ATM currently allows bit–rates of 45, 155, 622 and 2400 Mbit/s. The only bit–rate that is widely available is 155 Mbit/s, so an SDI signal at 270 Mbit/s must in most cases be compressed for transmission in ATM.

b) SDDI

The serial digital data interface (SDDI) is an extension of the existing SDI transmission system. SDDI data can convey video, audio and data in a variety of formats (e.g. SX, packetized and compressed data, ...). Theoretically, the SDDI is physically compatible with the basic SDI, although further studies are being conducted to verify its use in a real production environment. The SDDI allows 9–bit data words only, compared to the 10–bit word format of the SDI, in order to prevent the occurence of the reserved words in the SDDI data–stream.

1.4. Physical interfaces for digital component video signals

This *Section* describes the principal characteristics of the parallel and serial interfaces used to convey the digital component video signals discussed in *Section 1.1*.

1.4.1. Parallel digital interface

The parallel interface is described in detail in EBU document Tech. 3267 [S.3] and ITU–R Recommendation BT–656 [S.5]. New equipment is generally fitted with serial interfaces (*Section 1.4.2.*), but equipment using the parallel interface remains in service in many production facilities.

Ref. 4 and Ref. 5 show the most important features of the interface. *Ref. 4a)* shows the data signal in relation to the accompanying clock signal. The interface carries 8 <10> data signals and a separate synchronous clock. The clock period is 37 ns, which corresponds to a word–rate of 27 Mwords/s in the $C_B/Y/C_R/Y/...$ sampling structure described in *Section 1.1.1.b)*.

Ref. 4b) shows the eye pattern of the parallel data signal. The line receiver must correctly sense the binary data when the minimum values of the eye opening are 100 mV and 2 ns. The reference transitions of the clock should correspond exactly with the centre of the eye.

Ref. 4c) shows the link between an emitter–coupled logic (ECL) transmitter and receiver carrying one of the 8 <10> data lines or the clock. It can be seen that the signals are transferred symmetrically so they are insensitive to common–mode interference from external sources or via the ground connections. *Ref. 5* shows the pin assignment on the 25–pole D–type connector. The cable has male plugs at both ends and all equipment connectors (inputs and outputs) are female sockets.

The parallel standard requires a multi–core connecting cable (25 pole). The maximum cable length for shielded twisted–pair cable is about 50 m. This limit is due mainly to the cable capacitance, “bit skewing” (the effect by which the data bits are not all synchronized with the clock signal when they arrive at the receiver) and cross–talk.

The signal parameters which are defined in the standards documents and require to be measured during tests on parallel interfaces are discussed in *Chapter 4*.

1.4.2. Serial digital interface (SDI)

The serial digital interface is described in detail in ITU–R Recommendation BT–656 [S.5], EBU document Tech. 3267 [S.3] and SMPTE Recommended Practice 259M [S.6].

The word–rate of 27 Mwords/s of the parallel interface translates into a serial bit–rate of 270 Mbit/s in the SDI. The serial data word–length is 10 bits, even if the interface is carrying data with 8–bit resolution only. The serial data transmission order is least–significant bit (LSB) first.

A typical hardware configuration is shown in *Ref. 15*. The SDI transmitter includes a parallel–to–serial converter, a coder (scrambler) and a cable driver. In the receiver an equalizer regenerates the digital signal which suffers distortion caused by cable attenuation. The re–clocking device extracts the clock signal and the descrambler restores the original data.

The serial coder uses scrambled NRZI channel coding based on the following polynomial generator:

$$G1(x) * G2(x)$$

where:	$G1(x) =$	$x9 \oplus x4 \oplus 1$	to produce a scrambled NRZ signal
	$G2(x) =$	$x \oplus 1$	to produce the polarity–free NRZI sequence
	$\oplus$ =	logical exclusive–OR function.	

The scrambler performs two very important tasks:

– it helps to avoid the generation of very low–frequency components in the serial signal (although the scrambler may produce long sequences of logic “0”s which will not be removed by the G2(x) function);

– it increases the number of transitions in the serial signal (if there are too many consecutive logic “0”s in the data–stream, an excessive burden is placed on the PLL re–clocking system of the receiver).

The 9–bit scrambler (function G1(x)) can theoretically generate an infinite sequence of logic “0”s if the input signal consists only of “0”s. The longest sequence of “0”s in the digital signal is 39 (corresponding to a duration of about 144 ns), as occurs for example in the SDI check field (see *Section 6.3.2.*).

Conceptual diagrams of the scrambling, NRZ–to–NRZI coding, NRZI–to–NRZ decoding and descrambling functions are shown in *Ref. 16*.

As noted in *Section 1.1.2.*, data values in the range from 00.0_{hex} to $00.C_{hex}$ and from $FF.0_{hex}$ to $FF.C_{hex}$ are reserved for timing reference signals (TRS) and are not allowed for user or video data.

The interface is transparent to signals defined in ITU–R Recommendation BT.601, in either 8–bit or 10–bit representation. The video signal can be accompanied by up to 16 embedded digital audio channels conforming to the AES/EBU digital audio interface standard defined in EBU document Tech. 3250 [S.26], AES 3 [S.29] and SMPTE Recommended Practice 272M [S.32]. Video and ancillary data are carried in a single transmission link, in a time–multiplexed format.

Transmission over distances of up to about 300 m can be achieved using coaxial cable, without data regeneration, if automatic cable equalization is provided in the SDI receiver. Longer distances can be covered using fibre–optic transmission links (see *Section 1.4.3.*).

1.4.3. Optical interfaces

ITU–R Recommendation BT.656 [S.5] gives a tentative specification for a single–signal mono–mode optical interface. Further work within the SMPTE has led to the publication of SMPTE Standard 297M [S.10], covering the characteristics of transmitters, receivers, optical fibres and interface connectors for single–mode and multi–mode optical–fibre transmission.

At the present time, measurements on optical SDI systems can be carried out only in the electrical domain, before the electro–optic converter at the system input and after the opto–electric converter at the output. Therefore the performance specifications and measurement procedures are the same as described elsewhere in this document for the electrical parallel and serial interfaces.

Chapter 2

Measurements in the analogue domain

In many practical applications, digital component video systems are integrated with analogue systems operating with component ($Y/C_B/C_R$) or composite signals (e.g. PAL). This Chapter is concerned with the measurement of signal parameters in analogue equipment operating in conjunction with digital component systems, and in equipment used to convert between the analogue and digital domains.

2.1. A/D_{ser} and D_{ser}/A converters for video and audio signals

2.1.1. Purpose and constraints on performance

An A/D_{ser} converter serves to convert analogue component signals into a serial digital interface (SDI) signal; it comprises pre–filters and analogue–to–digital converters followed by a multiplexer and a serializer (parallel–to–serial converter)

A D_{ser}/A converter converts the SDI signal into the analogue component domain and comprises a de–serializer (serial–to–parallel converter), demultiplexer, digital–to–analogue converters and post–filters.

The performance of a converter depends on two main aspects: the design parameters (quantizing noise and related aspects) and the physical implementation.

a) Design parameters

The theoretical *quantizing noise* is dependent on the quantizing resolution:

Video:

$$S/N_{unweighted} = 10 \times \log\left(\frac{s^2}{12}\right) \quad \text{dB}$$

where: s = 100% / number of quantizing steps in the nominal video amplitude range.

This equation gives an S/N ratio (unweighted) of 57.64 dB for 8–bit video data words, or 69.65 dB for 10–bit video.

Audio:

$$S/N_{RMS} = 6n + 2 \quad \text{dB}$$

where: n = number of bits per sample.

The RMS S/N values derived from this equation are 98 dB (16–bit audio words), 122 dB (20–bit) and 146 dB (24–bit).

Static non–linearity errors affecting video converters will be of the order of 0.23% for 8–bit video and 0.06% for 10–bit video.

The theoretical minimum value of *ripple* affecting a video or audio signal will be equal to plus or minus one–half of the value corresponding to the least–significant bit (LSB).

b) Physical implementation

In some applications, and especially at the input of video and audio digital–to–analogue converters, the *jitter* should be less 1 ns (video) or 0.1 ns (16–bit audio). Jitter which exceeds these limits can cause linearity errors in the analogue domain (see *Appendix A*, [2] and [3]).

Inadequate D_{ser}/A converter design may lead to the generation of *glitches* in the output. No specifications have been issued on this topic, but all glitches should be as narrow and as small (i.e. of low amplitude) as possible. A narrow pulse of large amplitude is more easily eliminated than a wider and smaller one.

In both D_{ser}/A and A/D_{ser} converters the *converter non–linearity* should be maintained within the limits of one LSB.

Interference from the digital domain into the analogue domain circuitry or wiring may reduce the signal–to–noise ratio.

Finally, pre– and post–filters associated with D_{ser}/A and A/D_{ser} converters, defined in [S.1]) may cause *frequency response* and *group delay* errors.

It should be noted that even in A/D_{ser} converters which have the prescribed pre–filter characteristics, *aliasing* can occur. This is due to the effect of clipping of video signal levels at the A/D_{ser} processor, in situations where these levels exceed the headroom. The short transitions times associated with this clipping process, which occurs after the pre–filter, generate frequency components extending above the Nyquist limit and therefore produce aliased video signals at the output. The problem can be solved by placing an analogue limiter before the pre–filter.

2.1.2. Measurements

Specifications

Specifications for A/D_{ser} and D_{ser}/A converters are given in ITU–R Recommendation BT. 601.

Measurement equipment

The performance of A/D_{ser} and D_{ser}/A converters is verified using a test–signal generator with both analogue and SDI outputs, an SDI video analyzer and an analogue component video analyzer.

Three test patterns are required:

– colour bars;

– a variable flat field;

– a ramp (see ITU–R Recommendation BT.801 [S.33]).

Measurement conditions and procedures

Test methods and parameters are described in EBU Technical Information I15 [S.36]. The basic measurement configurations are shown in *Fig. 1*.

*A/D_{ser} converters (*Fig. 1a)*)*

Analogue test signals are fed to the A/D_{ser} converter and the digital signals produced by the converter are analyzed in the data domain. High–precision test signals are required simultaneously in the serial digital and the analogue domains. The comparison between the digital output of the generator and the digital output of the A/D_{ser} converter is made in the digital domain.

For error evaluations, and test patterns or programme material can be used.

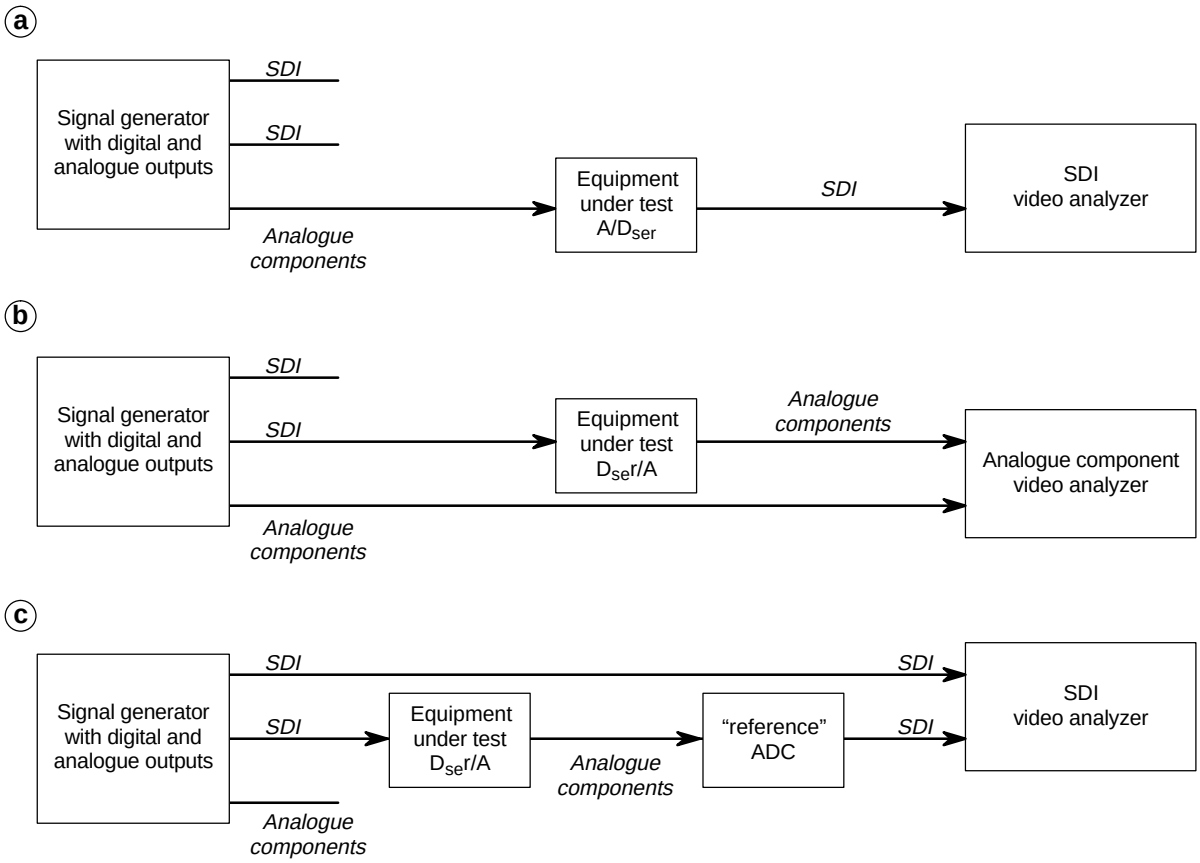


Fig. 1 – Block diagrams of D/A and A/D converter measurement configurations.

D_{ser}/A converters (Fig. 1b)*)*

An SDI signal is fed to the converter and the signal delivered at the output is analyzed in the analogue domain using an analogue component analyzer.

Combination of a D_{ser}/A converter and an A/D_{ser} converter (Fig. 1c)*)*

An SDI signal is fed to the first converter and the signal delivered by the second converter is analyzed in the digital domain.

The measurement and measurement methods used for isolated D_{ser}/A and A/D_{ser} converters are also applicable to converter combinations.

2.2. Analogue video before and after digital processing

2.2.1. Analogue video signal level

Specifications

The *Y* signal has limits of 0 and 700 mV.

The C_B and C_R signals have limits of ± 350 mV, centred on 0 mV.

For further details see [S.20], *Ref. 7* and *Ref. 8*.

2.2.2. Analogue rise and fall times

The luminance (Y) signal bandwidth is 5.75 MHz and the rise–time (from 10% to 90% of a 2–T Blackman[2] transition) should not be less than 150 ns.

The bandwidths of the C_B and C_R components are 2.75 MHz, with rise–times (10% to 90%) not exceeding 300 ns.

These specifications may be compared to those given for the data domain (*Section 3.1.2.*).

2.2.3. Picture position relative to the analogue synchronization pulse

Measurements should be made to verify that the timing relationship between a given point in the picture signal and the analogue synchronization is constant through the whole analogue–digital–analogue chain.

In television, two types of picture position errors must be considered:

– picture position relative to the line synchronization pulse (delay $<$ 64 µs);

– vertical picture position relative to the picture start (64 µs $\geq$ delay $<$ two fields).

Specifications

The start of the active analogue picture (50% level) is 10.5 µs after the timing reference t_o (this timing reference is at the 50% amplitude point of the leading edge of the line synchronization pulse).

There are 132 samples from the analogue line synchronization pulse to the start of the digital active line. The sampling frequency is 13.5 MHz, so the duration of those 132 samples is 9.778 µs (132×10^3/13.5 ns).

2. The Blackman pulse is a 2–T pulse whose frequency spectrum lies entirely within the specified bandwidth (5.75 MHz in this case). The spectrum of a conventional 5 MHz 2–T pulse extends partly beyond the 5 MHz bandwidth [12].

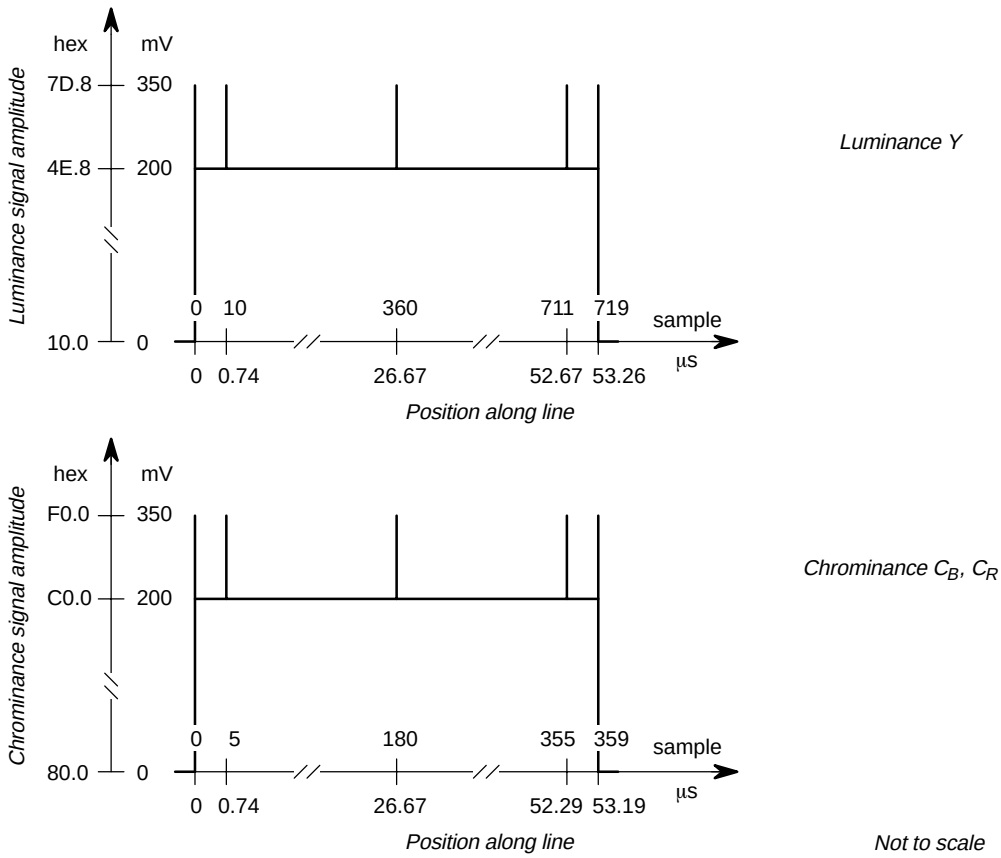


Fig. 2 – Test signals for picture position measurements.

Measurement equipment

Picture position is verified with an analogue video oscilloscope and a test pattern generator. This generator produces timing pulses on a pedestal corresponding to the waveforms shown in *Fig. 2* in every line of the active picture, and white level throughout lines 23, 310, 336 and 623. The timing pulses are grey–level words as Y samples 0, 10, 360, 711 and 719 and the corresponding chrominance samples 0, 5 180, 355 and 309. The pattern can be used in both the analogue and digital domains.

Measurement procedure

The test pattern is fed to the input of the digital–to–analogue converter or SDI–to–PAL converter under test, and the converter output is displayed on the oscilloscope. A picture monitor can be used for qualitative tests.

Four aspects of the picture position can be verified:

– *Vertical blanking:* In the analogue domain there should be half–lines in lines 23 and 623, and full lines in lines 310 and 336. In the digital domain, there should be full lines in lines 23, 310, 336 and 623.

– *Horizontal blanking:* In the analogue domain, two vertical lines should be visible, one at the beginning of the active line, the other at the end of the line. In the digital domain four vertical lines should be visible, two at each end of the active line.

– *Vertical picture position:* If this position is correct a one–and–a–half line white border will be visible across the top and bottom of the active picture area, when displaying the analogue signal on a picture monitor. In the case of a digital signal, the borders should fill two lines.

  A vertical picture position error is indicated by a horizontal offset of the white lines. In the case of an error of several lines, the white border will disappear into the vertical blanking interval.

  An offset of between one and two fields can be detected as a change in the length of the vertical blanking area.

– *Horizontal picture position:* If this position is incorrect, the amplitudes will be different at each end of the line. The vertical bar in the centre of the active line must be 36.49 µs after the leading edge of the analogue line synchronization pulse.

2.2.4. Video delay time measurements

Measurement equipment

Video delays in the analogue domain are measured in the analogue domain using an oscilloscope and a digital–to–analogue converter.

It is important to be aware that delay time measurements made using a digital–to–analogue converter can give erroneous results. This is because some precision D/A converters have an additional crystal–controlled phase–locked loop (PLL) operating at 27 MHz which, under certain circumstances, can lead to undefined delay times. Errors of ± 74 ns can occur.

If, for example, the D/A converter is connected after a switching matrix, the delay time differences of the switched input signals will determine how the D/A converter runs in. If a signal is switched through a matrix to the converter, the converter locks to this signal. In most cases, a signal is subsequently switched will still run–in with the reference delay time if its offset is within the range ± 15 ns.

If the offset is larger than this, the run–in of the D/A converter will be undefined. Jumps ranging from –111 ns to + 74 ns have been observed in practical installations and these will affect the operation of subsequent equipment.

Simple D/A converters with an L/C PLL will generally run–in in a reproducible manner.

The suitability of the D/C converter to be used for delay time measurements should therefore be assessed before the measurements are taken.

a) Measurement of delays of less than one line

Measurement equipment

Video delays of less than one line–period are measured using an oscilloscope and a D/A converter.

Measurement procedure

The equipment is connected as shown in *Fig. 3*.

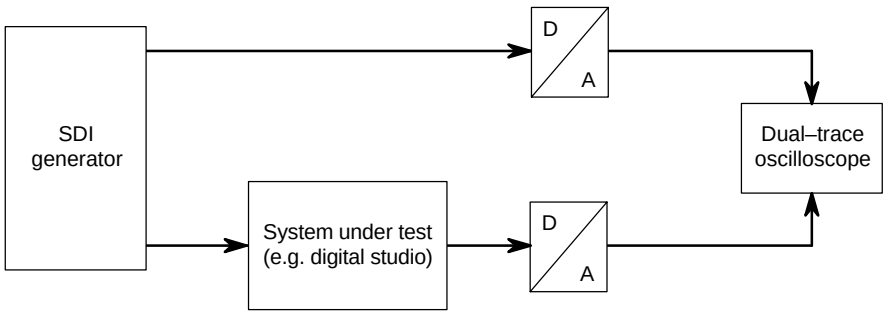


Fig. 3 – Connection of equipment for measurement of video delay time.

Presentation of results

The video delay is recorded in microseconds.

b) Measurement of delays exceeding one line ("vertical" delays)

Measurement equipment

Delay times are measured using two test signal generators and either an oscilloscope or a delay–time analyzer.

One test signal generator delivers a normal SDI signal. The other provides a PAL signal containing a field identification sequence. This may take one of two forms:

– Every 8th field (or every 32nd field) contains a white horizontal bar starting at, for example, line 200 and extending to the end of the active field. The other 7 (31) fields are black.

– Successive fields of an 8–field sequence delivered by a programmable PAL test–signal generator contain a full–field pedestal whose level is related to the position of the field in the sequence (field 1 – black; field 2 – 100 mV; field 3 – 200 mV; etc.), as shown in *Fig. 4*.

The delay time analyzer is a specially–designed instrument for the automatic measurement of the relative timing of PAL, analogue component and SDI signals. It is fed with signals from the sources to be compared and displays the timing difference in units of fields and lines. It should be possible to measure negative delays of up to about 100 lines.

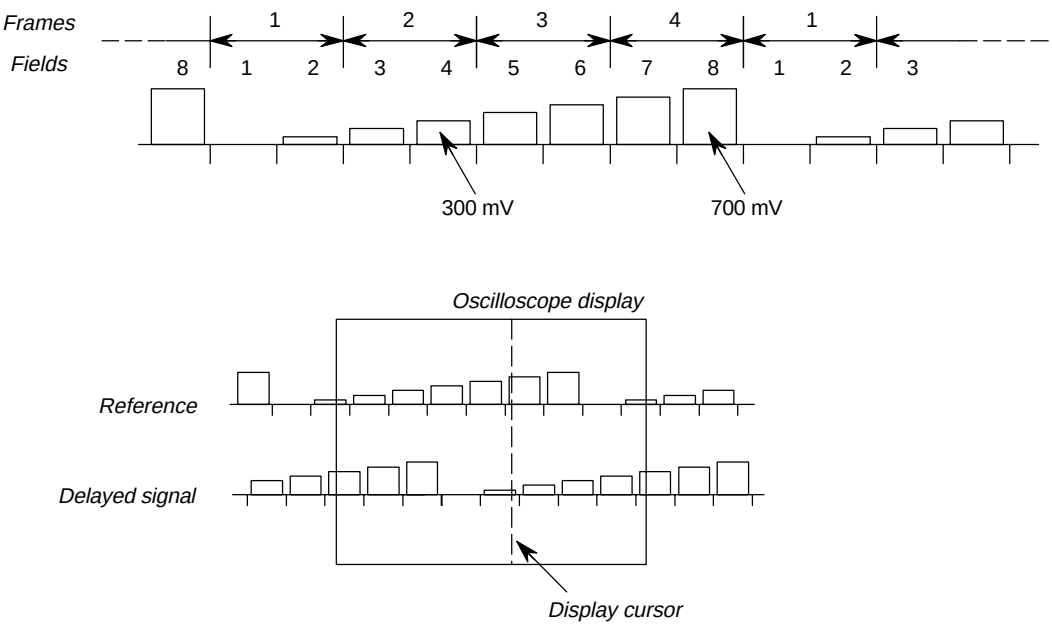


Fig. 4 – Vertical delay measurement using a programmable PAL test signal generator.

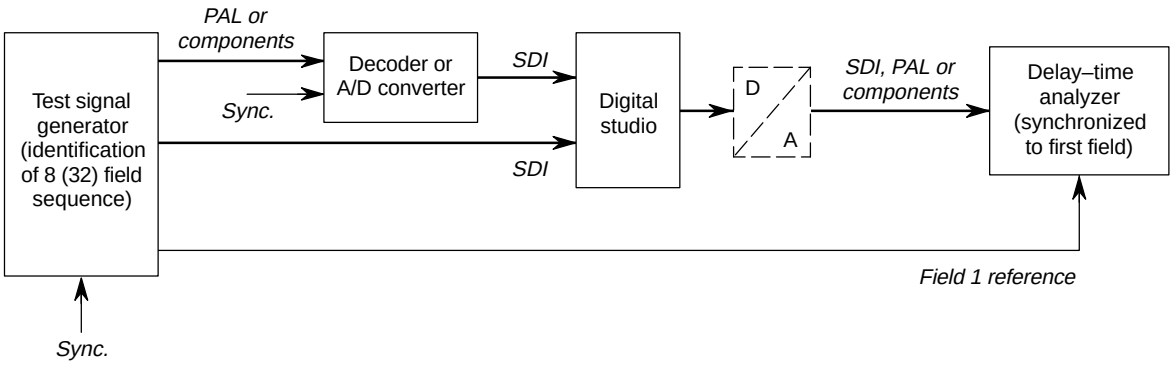


Fig. 5 – Video delay measurement in a digital studio.

Measurement procedure

Two methods may be used:

The first method uses the equipment arrangement shown in *Fig. 3*, with the oscilloscope synchronized to the master clock of the studio, and the test signal shown in *Fig. 4*. The delay can be identified by means of the different pedestals in each field of the test signal.

The second method uses the test equipment arrangement shown in *Fig. 5*. The delay is read directly from the delay time analyzer display.

Note:

All A/D converters in the studio – at the outputs of analogue signal generators and sound and picture signal sources – are synchronized by a single synchronization signal. A/D converters, like digital sources, have a run–in characteristic similar to that of D/A converters. Consequently a ± 74 ns delay time uncertainty can occur. This means, for example, that the A/D and D/A converters will run–in in a different way every time the main power switch of the studio is turned on.

2.2.5. Luminance/chrominance delay

Specifications

There is no formal specification for the relative timing of analogue luminance and chrominance components. EBU Technical Information I15 [S.36] notes that the maximum timing difference between should not exceed ± 10 ns.

Measurement equipment

Luminance/chrominance delay is measured using an analogue test–signal generator delivering colour bars or a pulse (8T or 10T), or a “bow–tie” signal, in association with a precision D/A converter and an analogue component video analyzer.

Measurement procedure

The SDI test signal is fed to the equipment under test and the analogue output is examined with the video analyzer.

Presentation of results

The time differences, in nanoseconds, between Y and C_B, Y and C_R and C_R and C_B should be recorded in the test report, together with a note of the test signal used.

2.2.6. Switching point of a video switching matrix

Specifications

SMPTE Recommended Practice RP 168 [S.24] indicates that a video switching matrix should switch in line 6 or line 319, in a “window” from 25 to 35 µs after the line synchronization pulse (see *Ref. 14*).

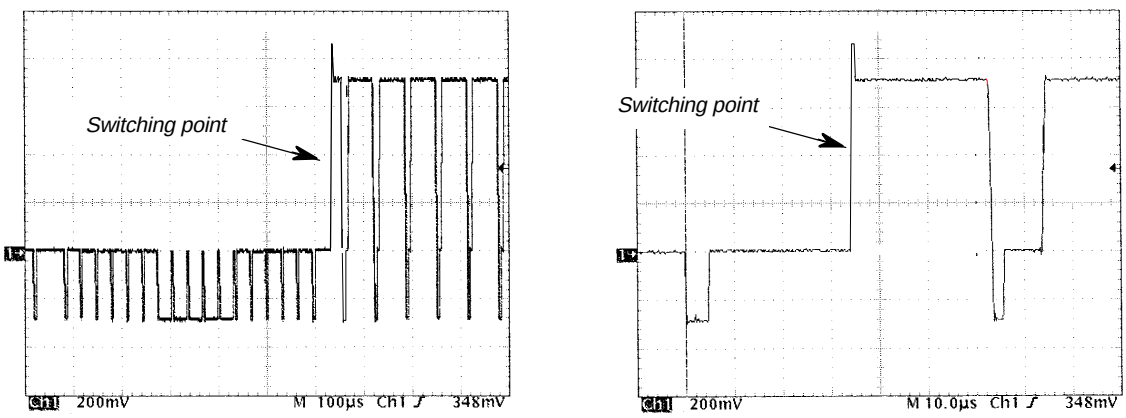
Measurement equipment

The verification of switching requires the use of a D/A converter which is transparent to the complete vertical–blanking interval, and a digital oscilloscope which can store several lines and has a single–shot trigger mode.

Two test signals are needed:

– one with black level in each line;

– one with white level in each line (or at least in lines 6 and 319).



Coarse measurement to determine switching line number.

Fine measurement (with horizontal expansion) to determine timing relative to line synchronization pulse.

Fig. 6 – Examples of oscilloscope displays of video matrix switching.

Measurement procedure

The test signals are fed to two inputs of the matrix, and the black signal is selected to the matrix output. This signal is fed to the oscilloscope via the D/A converter. The oscilloscope trigger is set to “active” and the trigger level set to 50% of the amplitude of an analogue white signal level. The trigger position should be moved to about 90% of the horizontal display width of the oscilloscope.

The matrix is then switched to connect the white signal to the output. The switching point is identified as the point where the oscilloscope display shows a change to white level (see *Fig. 6*).

Presentation of results

The line number and the time from the leading edge of the analogue line synchronization pulse to the switching point are recorded in the test results.

2.2.7. Colour gamut

The colour gamut is the range of colours that can be displayed within the triangle defined by the specified primary chromaticities for a given television system. In terms of RGB signal components, it is possible to display any colour whose R, G and B values each lie between 0 and 100% of the peak signal level (see *Fig. 7a*).

This can be, almost certainly, guaranteed when the originating source of the picture is a television camera or telecine irrespective of the fact that the original RGB signals may be converted at a later stage to a different component system. In contrast, when signals are originated in a component system involving a luminance signal and two chrominance signals it is quite easy to have the situation where an illegal signal is created. This can occur with graphics origination, electronically–generated test signals and in special effects systems. When these components are converted to R, G and B signals for display, the signal levels can extend outside the range from 0 to 100%, thereby creating a colour, outside the display gamut, which cannot be displayed faithfully. This situa-

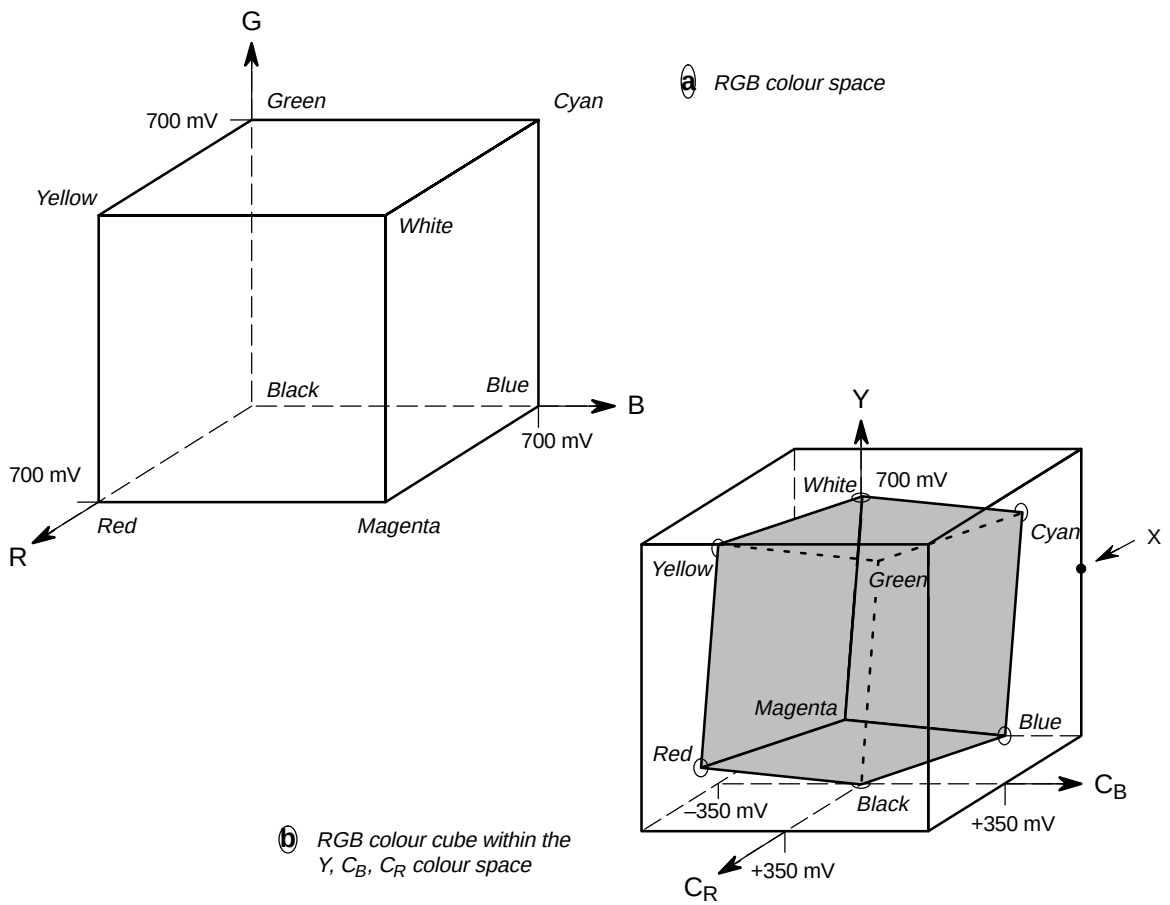


Fig. 7 – Colour gamut.

tion is represented by the volume outside the shaded cube in *Fig. 7 b)*, such as the point marked X which represents an illegal colour with the coordinates Y = 350 mV, C_B = 350 mV, C_R = –350 mV.

It is not easy to define the luminance and colour difference signal levels that will create an illegal colour in the RGB or PAL domains. This is because, in real life, luminance is not an independent quantity and all colours cannot exist at all luminance levels. To exercise adequate control over the colour gamut, it is therefore necessary to monitor signals in the RGB domain and ensure levels do not go negative or above 100% values.

Waveform monitors are available for this purpose. These usually have two indicator lights to warn about out of gamut signals; the "POS" light will switch on when one or more of the RGB signals exceeds the peak level and the "NEG" light will switch on when a negative value is detected. The violated areas can be shown on a picture monitor.

Note: Methods of achieving a wider colour gamut are presently being considered for use in advanced television systems. One method is to allow RGB signals to go negative and above 100%, with any increase in range being restricted so that coded signals still fit within the chrominance channels defined in ITU–R Recommendation BT.709 [S.16]. In such a case an out–of–gamut signal would be created if decoding resulted in RGB signals which went outside this new range of levels.

Specifications

Pending the development of full specifications for PAL, SECAM and NTSC, and for advanced systems, it seems reasonable to stay in the RGB domain within the video level limits of 0 – 103%.

Measurement equipment

Colour gamut can be verified with an oscilloscope or a waveform monitor with gamut indicators.

Measurement procedure

RGB signals are monitored at the point of interest to ensure that for any colour (scene colour or computer–generated graphics colour) the levels are not outside the specified range.

2.2.8. Picture aspect ratio conversions (4:3 to 16:9 and vice versa)

If an analogue PAL signal in 4:3 aspect ratio is converted to an SDI signal, and this is converted to a 16:9 aspect–ratio picture, PALplus artifacts are likely to appear if the signal is converted back into 4:3 aspect ratio.

An appropriate measurement method is under study.

2.2.9. Analogue audio before and after A/D – D/A conversion

Specifications

The performance limits for the EBU/AES digital audio interface are laid down in EBU document Tech. 3250 [S.26][S.27].

Measurement procedures

A number of measurements on analogue audio which have been used successfully over the years, covering levels, frequency response, signal–to–noise ratio, total harmonic distortion and phase and level differences between channels. These are still valid on modern audio circuits.

For the digital part of the circuit between the A/D and D/A converters, additional tests are described fully in AES 17 [S.42]. Some of these tests serve to quantify the artefacts caused by the processes of sampling, quantizing, filtering and the number of bits. Others include the assessment of clock jitter, the suppression of aliasing, out–of–band and intermodulation products, overload and delay behaviour, idle channel and intermodulation noise, and harmonic distortion and noise as functions of frequency or level.

Experience has shown that these tests do not always give a true measurement of system performance, particularly in systems employing coding or bit–rate reduction. A new method of measurement involving the use of source material based on critical real programme segments has been proposed [12]. A project is being set up to further this work and one of the aims is to build up a library of suitably critical programme material.

Chapter 3

Measurements in the data domain

This Chapter describes methods for the verification of different aspects of the data carried in the electrical waveform of the serial digital interface.

3.1. Video signal

3.1.1. Video signal level

Specifications

Ref. 7 shows the boundaries of the luminance (*Y*) component of 8 and 10–bit digital video signals. The nominal video signal comprises 220 <877> quantizing levels, with black level corresponding to the value 16_{dec} (64_{dec}) and nominal white level corresponding to the value 235_{dec} <940_{dec}>. An upper headroom, above the nominal peak video level of 700 mV, extends over a range of 19 <79> quantizing steps. A lower headroom, below the nominal minimum video level of 0 mV, covers 15 <60> quantizing steps.

Ref. 8 shows the boundaries for the chrominance channels, (C_B, C_R). The nominal video signal comprises 225 <897> quantizing levels. Zero signal level corresponds to the value 128_{dec} <512_{dec}>, the maximum positive level corresponds to level 240_{dec} <960_{dec}> and the maximum negative level corresponds to level 16_{dec} <64_{dec}>. Positive headroom extends over 14 <59> quantizing steps and negative headroom extends over 15 <60> quantizing steps.

Measurement equipment

The measurement of video signal levels in the data domain requires the use of a test–signal generator which is able to generate both legal and illegal 10–bit test signals, and deliver them via 8 and 10–bit parallel interfaces and in the 10–bit SDI format.

The measurements are made with a digital video analyzer which is able to display the samples in the data domain.

3.1.2. Rise and fall times

Specification

There is no specification for the rise and fall times in the data domain, although the overall system bandwidth of the digital system is specified in ITU–R Recommendation BT.601 [S.1].

ITU–R Recommendation BT.801 [S.33], describing test patterns for digital component video systems, indicates a rise–time of 150 ns for the luminance component and 300 ns for the chrominance components; all the transitions have Blackman characteristics.

At the time of writing, the SMPTE was planning to issue a Recommended Practice concerning rise and fall times in the data domain, as follows:

Luminance: 0 dB bandwidth = 5.75 MHz, corresponding to a minimum transition time of 174 ns (from 10% to 90% of a $\sin^2$ transition);

Chrominance: 0 dB bandwidth = 2.75 MHz, corresponding to a minimum transition time of 364 ns (from 10% to 90% of a $\sin^2$ transition).

To facilitate measurements of transition times, it should be possible to adjust the shift the window of the oscilloscope relative to the half–amplitude points of the transitions.

Measurement equipment

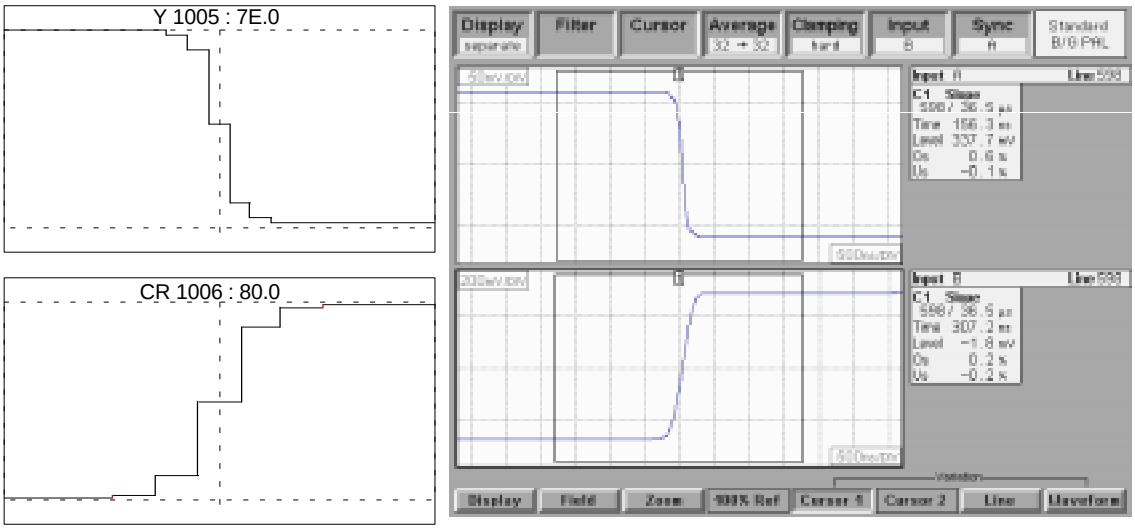
Rise and fall times are measured using a digital video analyzer which is able to measure the parameters of each pixel of the picture.

Measurement conditions and procedure

The SDI signal is connected to the digital analyzer. The analyzer should be able to calculate an equivalent analogue signal wavefront from the video data, applying the filter characteristics of ITU–R Recommendation 601, and display it on the screen, as shown in *Fig. 8*.

100% colour bars with rise and fall times in accordance with standards.

Unfiltered digital waveform *Analogue waveform after ITU–R 601 filtering*



100% colour–bars with excessively fast rise and fall times

Unfiltered digital waveform *Analogue waveform after ITU–R 601 filtering*

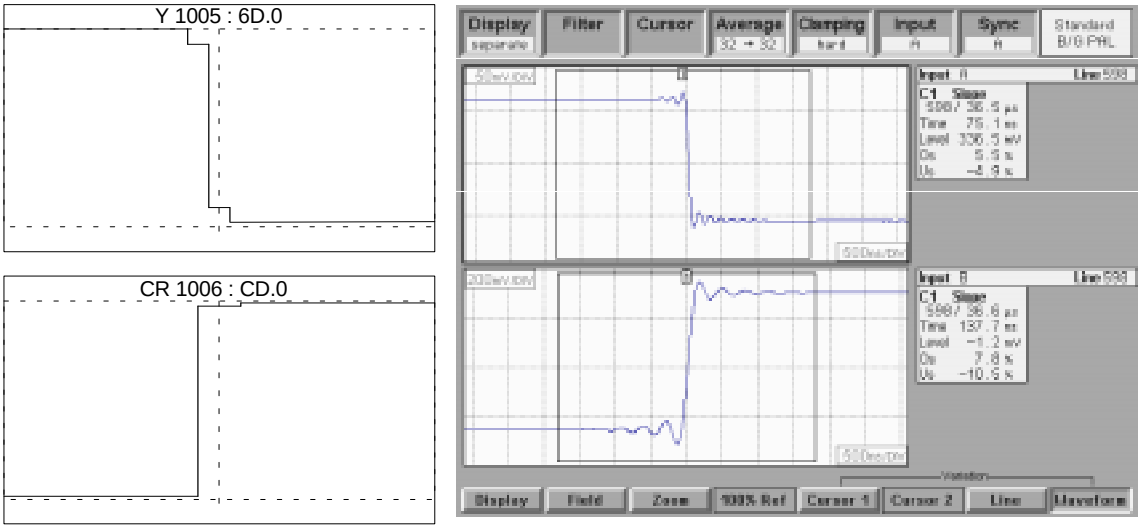


Fig. 8 – Measurement of digital rise and fall times, and analogue overshoot and ringing.

Presentation of results

The results are recorded in the measurement report in terms of the time, in nanoseconds, between the 10% and 90% amplitude points.

Note:

In a digital system it is possible to generate a signal with a transition from 0% to 100% in the time between two successive samples. This would result in a transition time of less than 74 ns in the luminance channel (or less than 148 ns in the chrominance channels); such transitions would be outside the permissible bandwidth of the standard and the post–filter following a digital–to–analogue converter would produce large overshoots (see *Fig. 8, bottom).*

3.1.3. Picture position, relative to timing reference signals (TRS)

Specification

The SMPTE has issued a specification defining the position of the picture relative to the timing reference signals [S.25]. The timing relationship of the video data to the TRS must be maintained, as defined in *Ref. 2* and *Ref. 6.*

Measurement equipment

Picture position is measured using a digital video analyzer and a test signal having a vertical structure whose horizontal position is known. A colour–bar signal as described in ITU–R recommendation BT.801 [S.33] is suitable.

Measurement procedure

The signal is fed to the analyzer an the sample positions are verified.

3.1.4. Luminance/chrominancedelay

Specification

No specification is given for the luminance/chrominance delay in the data domain, but from comparison with the specification applicable in the analogue domain, a maximum timing difference between the luminance and chrominance components should not exceed 10 ns. Tracking between the two chrominance components should be better than 5 ns.

Measurement equipment

Luminance/chrominance delay is measured using an SDI test–signal generator delivering a colour–bar signal conforming to ITU–R Recommendation BT.801, and an SDI video analyzer fitted with ideal software filters which give an analogue display corresponding to the digital waveform.

Measurement procedure

The video analyzer is fed with the SDI signal from the equipment under test.

Presentation of results

The time differences between the three components should be recorded in the measurement report ($Y - C_B$, $Y - C_R$, $C_B - C_R$).

Notes:

It is not likely that a luminance/chrominance delay will occur in the digital domain, although signals originated in the analogue domain and transferred via an analogue–to–digital converter (ADC) into the digital domain may have errors. These errors may be introduced in the analogue source, in the signal path or in the A/D conversion process. The measurement procedure described above will assist in determining the cause of such errors.

It is difficult to measure luminance/chrominance delays in the data domain because of the 37 ns sampling period. A timing difference of, for example, 10 ns, would show as an amplitude difference in a certain sample. To facilitate measurements, it is advisable to use the SDI video analyzer in a mode which uses ideal software filters to create a display of an equivalent analogue waveform.

3.1.5. Forbidden data words

The following data words are reserved for synchronization purposes (TRS and ancillary data signal preambles):

8–bit systems	00_{hex}	and	FF_{hex}
10–bit systems	$00.x_{hex}$	and	$FF.x_{hex}$

The synchronization codes for 10–bit systems are not clearly defined. In practical equipment, the following codes are used:

00.0_{hex}, $00.C_{hex}$ and $FF.0_{hex}$ $FF.4_{hex}$, $FF.8_{hex}$ and $FF.C_{hex}$

Measurement equipment and procedure

Verification for forbidden data words is done using a digital video analyzer, fed from the SDI output of the equipment under test.

3.2. Timing reference signals (TRS)

Specification

The timing reference signal specifications are given in EBU document Tech. 3267 [S.3] (see *Ref. 6*).

The XY words (fourth word of the TRS) in successive lines of the SDI signal should be as follows:

Lines			SAV	EAV
23	to	310	$80.X_{hex}$	$9D.X_{hex}$
311	to	312	$AB.X_{hex}$	$B6.X_{hex}$
1	to	22	$AB.X_{hex}$	$B6.X_{hex}$
313	to	335	$EC.X_{hex}$	$F1.X_{hex}$
336	to	623	$C7.X_{hex}$	$DA.X_{hex}$
624	to	625	$EC.X_{hex}$	$F1.X_{hex}$

Measurement equipment

Timing reference signals are verified using a digital video analyzer.

Measurement procedure

The TRS of every line in a full video frame should be compared with the values in the table above.

Presentation of results

A list of all TRS sequences which are not correct should be recorded in the measurement report, as shown in the following example:

line 313	SAV expected:	$EC.0_{hex}$	detected:	$AB.0_{hex}$
line 1	EAV expected:	$B6.0_{hex}$	detected:	$F1.0_{hex}$

3.3. Ancillary data

3.3.1. AES/EBU audio signals

The full measurement of digital audio signals is beyond the scope of the present document. Reference should be made to AES 17 [S.42].

An AES/EBU digital audio analyzer can be used to investigate the ancillary data groups to verify the plausibility of the data they are carrying. The channel status bits of the audio sub–frames should be checked to ensure that they are set for the intended system operation, and that they have not been modified inadvertently as they pass through the digital chain. A table showing the channel status information is shown in *Ref. 17*.

3.4. Conversion between 8–bit and 10–bit representations

3.4.1. Conversion from 10–bit to 8–bit representation

The SDI operates with 10–bit data words and to maintain a high degree of compatibility it must operate correctly when it is used to carry 8–bit signals. EBU document Tech. 3267 specifies that the two least–significant bits (LSB) are set to “0” or “1” when carrying 8–bit data.

It should be noted that 10–bit equipment which receives an 8–bit signal cannot determine whether the two LSBs are “random” bits or true signal bits. A 10–bit system carrying 8–bit data should have the two LSBs set specifically to “0” or “1”. They should not be left floating.

If it is necessary to convert from 10–bit to 8–bit format, for requirements not involving the SDI but, for example, linked to signal processing, rounding or truncation techniques can be applied.

Rounding is the removal of the two LSBs after a correction has been applied.

Truncation is the simple removal of the two LSBs.

Both methods cause an increase in the quantization noise, to the level typical of an 8–bit system. Truncation introduces a DC error equal to one–half of an 8–bit quantization level. The AC noise is the same as that obtained with rounding.

With suitable pathological signals, it is possible to see contouring errors in areas of the picture which are of uniform brightness. Whether rounding or truncation is used, the contouring disturbance can be reduced by introducing dither, as either a random or a fixed pattern, before re–quantization. The dither causes the eighth bit to be artificially modulated. The effect on a slowly–varying signal is equivalent to a doubling of the number of quantization levels, leading to a much–reduced contouring effect and better subjective quality.

The use of dither in bit reduction processes has been known for many years but has not been widely implemented. The method described in [14] is the most suitable.

Measurement equipment

The conversion from 10–bit to 8–bit data formats can be verified using a 10–bit SDI signal generator, a serial–to–parallel converter and an oscilloscope.

Measurement procedure

The type of dither used in a 10–bit to 8–bit conversion process, and the quality of the process, requires the use of a 10–bit signal generator with the possibility of implementing a continuously–variable pedestal, with manual and automatic control, corresponding to each quantizing level.

The pedestal (grey) signal is injected at the input to the equipment under test. The signal delivered at the output is converted to parallel form and the behaviour of the eighth bit is observed on the oscilloscope as the pedestal level is varied.

In this way it is possible to check the following three features of the 10–bit to 8–bit conversion process:

– presence of truncation only;

– presence of rounding only;

– insertion of dither.

It can also be seen if the noise level on the analogue source signal was large enough to cause a natural dither effect.

3.4.2. Conversion from 8–bit to 10–bit representation

If a parallel–to–serial converter is fed with a parallel signal carrying only eight active bits of video data, the serializer must be able to identify this condition and add the necessary data to convert the 8–bit input into a valid 10–bit serial format.

3.5. Most important measurements in the SDI data domain

Table 2 lists the most important measurements that should be carried out on all SDI equipment to ensure proper functioning.

Table 2 – Required measurements in the data domain (SDI).

Measurement	Described in *Section*
Timing reference signal (TRS) check	*3.2.*
Verification for forbidden data words (reserved codes)	*3.1.5.*
Bit–error ratio (BER) and error detection and handling (EDH)	*6.4.*
Number of active bits (8/10)	*3.1.1.*
Digital signal levels (hex, dec and mV)	*3.1.1.*
Rise and fall–times	*3.1.2.*
Picture position position relative to the TRS	*3.1.3.*
Ancillary data (including type / length indications)	*3.3*
Luminance/chrominance delay	*3.1.4.*
Propagation delay through SDI equipment	

Chapter 4

Measurements in the physical domain

This Chapter describes measurement procedures for the principal physical characteristics of the parallel and serial interfaces.

In the following Sections, the description of each measurement begins by recalling the relevant specifications, taken from the standards documents presented in *Chapter 1*.

4.1. Parallel interface

4.1.1. Signal level and DC shift

a) Specifications

Line driver

The maximum positive level on each of the symmetrical lines should be –0.8 V

The maximum negative level on each of the symmetrical lines should be –2.0 V

The maximum peak–to–peak signal amplitude can be derived by subtracting the maximum positive value from the maximum negative value; it should be between 0.8 and 2.0 V.

The common–mode voltage between each of the symmetrical lines and ground should be –1.29 V ± 15%.

Line receiver

The line receiver must correctly sense the binary data when a random data sequence produces the conditions represented by the idealized eye diagram shown in *Ref. 4b)* at the data detection point.

The receiver should operate with a minimum input signal of 100 mV_{p-p}, and with data transitions within ± 11 ns of the reference transition of the clock.

b) Measurement equipment and conditions

The measurements can be carried out with an oscilloscope having a bandwidth in excess of 150 MHz[3].

The twisted–pair line must be terminated with a 110 Ω resistor.

c) Measurement procedure

When measuring the signal amplitudes on each of the symmetrical lines and ground, the maximum positive level should be –0.8 V with respect to ground, and the maximum negative level at –2.0 V. The data cross–over point (close to 50% of the transition), should be at –1.4 V.

3. See *Section 4.2.3.b)* for further discussion on oscilloscope bandwidths.

Measurements between the symmetrical lines should be made using two probes at the same time. This also allows examination of the eye diagram, if one channel is set to “invert” and “add”.

It should also be verified that all 8 <10> bits of the data stream are present and that they change independently.

4.1.2. Rise and fall times

a) Specifications (line driver)

The rise and fall times between the 20% and 80% amplitude points, on both symmetrical lines and with a 110 Ω termination, should be less than 5 ns.

The difference between the rise and fall times must not exceed 2 ns.

b) Measurement equipment, conditions and procedure

Rise and fall times can be verified using the techniques presented for signal amplitude measurement in *Section 4.1.1*.

4.1.3. Timing

a) Specifications

Line driver

The clock period for the 625–line system is 37 ns.

The pulse width is 18.5 ± 3 ns.

The positive–going edge of the clock pulse should coincide, with a tolerance of ± 3 ns, with the middle of the data signal pulses, as shown in *Ref. 4a)*.

Line receiver

The clock signal is sent through the parallel interface along with the 8 <10> data bits. At the receiver, the mid–point of the eye–diagram of each data–stream should coincide, with a tolerance of ± 11 ns, with the transitions of the clock signal, as shown in *Ref. 4b)*.

b) Measurement equipment, conditions and procedure

The signal timing can be verified using the techniques presented for signal amplitude measurement in *Section 4.1.1*.

4.1.4. Jitter

a) Specifications (line driver)

The clock pulse width is 18.5 ± 3 ns.

The timing of individual rising edges of clock pulses (jitter) shall be within ± 3 ns of the average timing of these edges over a period of at least one field.

Note: This specification is appropriate and sufficient for the parallel interface but is not suitable as a source for clocking a parallel–to–serial converter or a digital–to–analogue converter because of the tighter tolerance that is required in the serial domain.

b) Measurement equipment, conditions and procedure

The measurement of jitter in the parallel interface can be based on the methods described for the serial interface in *Section 4.2.5.* and *Appendix A*, which include a full discussion of the problem of jitter measurement.

4.1.5. Impedance

a) Specifications

Line driver

The output impedance of the line driver should have a maximum value of 110 Ω.

Line receiver

The input impedance of the line receiver should be 110 ± 10 Ω.

b) Measurement procedures

Two methods may be used:

a) Output and input impedances may be measured with a network analyzer.

b) The output impedance can be measured with an oscilloscope. The line driver is connected to the high–impedance input of the oscilloscope and the data amplitude is measured. If an accurate 110 Ω termination is connected across the twisted–pair line the signal level should decrease to a maximum of one–half of the previously–measured data amplitude. The waveform should be examined to ensure that the eye opening is not excessively restricted with respect to the requirements shown in *Ref. 4b).*

4.1.6. Common–mode rejection

a) Specification (line receiver)

The line receiver must receive data correctly even if a signal degradation occurs on both lines as a result of interference.

The maximum common–mode signal between each terminal and ground should be ± 0.5 $V_{p–p}$, for any interfering signal in the frequency range from 0 to 15 kHz.

b) Measurement procedure

Immunity to the effects of an interfering signal can be examined on an oscilloscope. An interfering signal can be induced into the data lines by means of a transformer.

It is recommended also that a CRC[4] checksum device is used to detect any increase in data errors when interference is present.

Interference problems may be caused by poor installation practices rather than inadequate equipment design or equipment faults.

4. CRC: cyclic redundancy check

4.2. Serial interface

4.2.1. Precautions when making physical measurements on the SDI

The connection of test equipment such as an oscilloscope to a serial digital signal is very critical because of the frequency bandwidth involved. When making measurements on the SDI operating at 270 Mbit/s, the coaxial cable used to make such connections should be as short as possible (maximum 2 meters).

The best solution is to use an oscilloscope with an internal 75 Ω termination, although such equipment is difficult to obtain.

A more practical approach is to use a 75/50 Ω impedance converter designed for frequencies up to 500 MHz. The oscilloscope must be terminated internally with 50 Ω. These converters normally have an amplitude loss of up to 6 dB, so the results must be corrected accordingly.

It is also possible to use a 75 Ω through terminator; it should have a reflection loss of at least 15 dB at frequencies up to 500 MHz. The oscilloscope should be switched to "high–impedance" mode.

For critical measurements, the connection of test equipment to the serial signal should not be made with a normal 75 Ω termination using a T–piece.

The preferred method for measuring the amplitude, rise–time and overshoot of the serial digital signal is to use an oscilloscope with a bandwidth of 1 GHz, or special equipment intended for SDI measurements. The input impedance of the oscilloscope should be 75 Ω, with a return loss greater than 20 dB at frequencies up to 400 MHz.

Except where otherwise specified in the following Sections, a pseudo–random test signal, such as that provided by colour bars, should be used.

4.2.2. Output level and DC offset

a) Specifications

The peak–to–peak amplitude of the SDI signal should be 800 mV ± 10%.

The DC offset should not exceed ± 500 mV.

b) Measurement equipment and procedure

The SDI signal is connected to the vertical channel of an oscilloscope having a bandwidth of at least 150 MHz. The results are recorded, in millivolts.

Note: The amplitude of the SDI signal incoming to the receiver is the basis for operation of the automatic cable equalizer. If the signal at the sending end is incorrect, the length of cable which can be exploited correctly will be reduced because the automatic equalizer in the receiver always assumes that the transmitter is sending at the nominal level of 800 $mV_{p–p}$. If the sending level is not correct, over– or under–equalization may occur, and this may produce errors. In practice, any increase in sending level above the nominal level (even within the tolerance range allowed) may lead to errors (see also *Sections 4.2.9.* and *4.2.10.*)

4.2.3. Rise and fall times

a) Specifications

The rise and fall times, determined between the 20% and 80% amplitude points and measured across a 75 Ω resistive load, should lie between 0.75 ns and 1.5 ns[5]. The rise and fall times are shown in *Fig. 9*. The rise and fall times should not differ by more than 0.5 ns.

5. The SMPTE is expected to specify new limits for the rise–time and overshoot in the SDI.

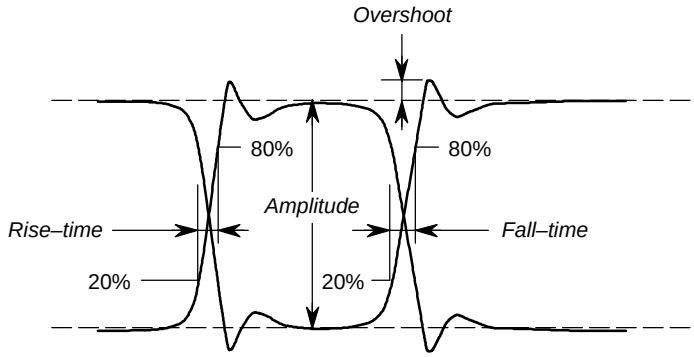


Fig. 9 – Rise–time and overshoots of the SDI waveform.

b) Measurement equipment and conditions

The SDI signal is connected using a cable no longer than 2 meters long, to the vertical channel of an oscilloscope having a bandwidth of 1 GHz, or a special SDI measurement test set. The oscilloscope is triggered from the SDI signal itself.

When measuring the rise–time of a serial signal with an analogue oscilloscope, it should be noted that if the oscilloscope bandwidth is less than 1 GHz the measurements will be in error owing to the low–pass filter characteristic of the oscilloscope input. The measured value should be corrected using the following formula:

$$T_a = \left(T_m^{\ 2} - 0.5T_s^{\ 2}\right)^{1/2}$$

where: $T_{a(20/80)}$ = true rise–time
$T_{m(20/80)}$ = measured rise–time
$T_{s(10/90)}$ = oscilloscope rise–time.

The factor of 0.5 compensates for the fact that the oscilloscope rise–time is given between the 10% and 90% amplitude points.

Examples: If the oscilloscope rise–time (10% to 90%) is 1.0 ns, a measured rise–time of 1.2 ns would indicate a real SDI waveform rise–time (20% to 80%) of 0.97 ns; a measurement of 1.6 ns would correspond to a real value of 1.44 ns.

In general, experience has shown that the increased accuracy obtained by using the above formula is lost in uncertainties when reading the oscilloscope trace. The suitability of any particular oscilloscope can be judged by using the formula:

$$T_s = \frac{0.35}{bandwidth}$$

where: $T_{s(10/90)}$ = oscilloscope rise–time.

4.2.4. Overshoot and overshoot symmetry

a) Specifications

SMPTE Standard 259M [S.6] specifies that the over– and under–shoot should be less than 10%.

No specification is given for the symmetry.

Overshoot is shown in *Fig. 9*.

b) Measurement equipment and conditions

The SDI signal is connected using a cable no more than 2 meters long, to the vertical channel of an oscilloscope having a bandwidth of 1 GHz, or a special SDI measurement test set. The oscilloscope is triggered from the SDI signal itself.

4.2.5. Jitter

For a full appreciation of this section concerning the measurement of jitter in the SDI, it will be necessary to be conversant with the concepts and principles described in *Appendix A*.

a) Specifications

ITU–R Recommendation BT.656 [S.5] specifies the jitter tolerance as follows:

> *"the timing of the rising edges of the data signal shall be between ± 10% of the clock period, as determined over a period of one line".*

This means that at 270 MHz, with a clock period of 3.7 ns, the maximum jitter should be within the limits of ± 0.37 ns (absolute value 0.74 ns).

This specification is under revision at the time of writing. SMPTE Recommended Practice RP 184 (1995 version) specifies parameters for jitter measurements and the proposed revision of SMPTE Standard 259M (January 1995 version) specifies the values for compliance with the standard:

timing jitter:	(frequencies from <10 Hz to 27 MHz)	$=0.2\ UI_{p-p}$
alignment jitter:	(frequencies from <1 kHz to 27 MHz)	$=0.2\ UI_{p-p}$

The revised SMPTE Standard specifies that the measurements should be taken using a colour–bar test signal, which produces a large number of transitions in the serial data–stream. The SMPTE Recommended Practice suggests that the SDI check–field, designed principally for tests on SDI receivers, is not suitable for jitter measurements. The specified measurement duration is 60 s (instead of one–line period, as specified in ITU–R Recommendation 656). The serial clock divider should not be set to divide by ten, so as not to be synchronized with the word rate, in which case word–correlated effects would be masked. Finally, although the specified jitter frequency ranges extend up to 27 MHz, jitter may occur at up to 54 MHz, with destructive effects on the SDI signal.

b) Measurement equipment, conditions and procedures

Five measurement methods are described in this Section, covering the various forms of jitter discussed in *Appendix A*.

1. Measurement of timing and alignment jitter using a clock extractor and oscilloscope

Measurement equipment

The method uses a clock extractor (see *Appendix A, Section A5.1.*) and an oscilloscope with a bandwidth of 500 MHz. A digital storage oscilloscope with infinite persistence is recommended.

Measurement procedure

The SDI signal is connected via the loop–through at the clock–extractor input, to the vertical channel of the oscilloscope. The oscilloscope is triggered from output 2 of the clock extractor (*Appendix A, Fig. A5*).

Timing jitter is measured with the clock–extractor bandwidth set to *B1 (Appendix A, Fig. A1).*

Alignment jitter is measured with the clock–extractor bandwidth set to *B2 (Appendix A, Fig. A1).*

If the jitter amplitude is greater than 1 UI, the clock divider should be switched into operation (division by the factor *n*).

Presentation of results

The clock–recovery bandwidth (*B1* or *B2*), the clock divider setting (*n*) and the jitter amplitudes should be noted in the measurement record.

Note: The disadvantage of this method using a clock extractor and oscilloscope is that individual jitter frequencies cannot be determined. If the jitter frequencies can be found, the source of jitter could be determined more easily. For example, if the predominant jitter frequency is 50 Hz (or multiples of 50 Hz), one possible cause of the jitter might be the power supply.

Methods 2 and 3 below allow the jitter frequency spectrum to be determined.

2. Measurement of the jitter spectrum using a clock extractor and spectrum analyzer

Measurement equipment

The method uses a clock extractor (see *Appendix A, Section A5.1.*) and a spectrum analyzer which should have a bandwidth of 500 MHz and a resolution bandwidth of 10 Hz.

Measurement procedure

Output 1 of the clock extractor (clock signal with original jitter) is connected to the spectrum analyzer, set to a resolution bandwidth of 10 Hz.

If the jitter amplitude is greater than 1 UI, the clock divider should be switched into operation (division by the factor *n*).

The sidebands of the clock frequency (phase noise) will correspond to the jitter frequencies, as shown in the example in *Fig. 10*.

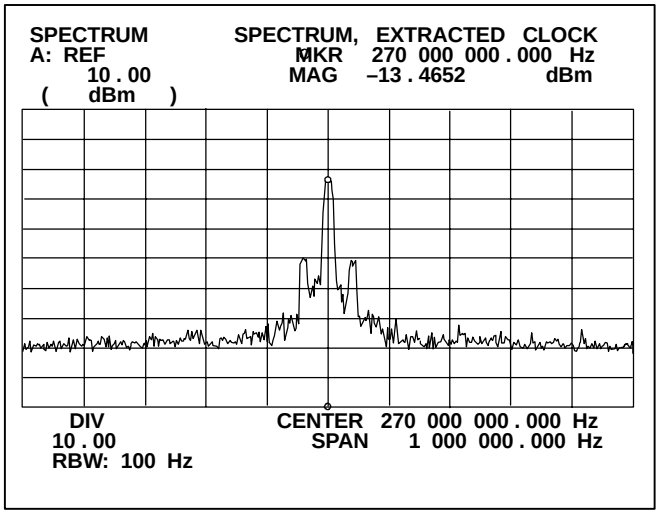


Fig. 10 – Example of spectrum analyzer display, showing jitter frequencies as sidebands of the displayed clock frequency.

Presentation of results

The dominant jitter frequencies and their amplitudes should be noted in the measurement record, together with the clock divider setting (*n*) and the resolution of the spectrum analyzer.

3. Measurement of the jitter spectrum using a clock extractor and phase demodulator

Measurement equipment

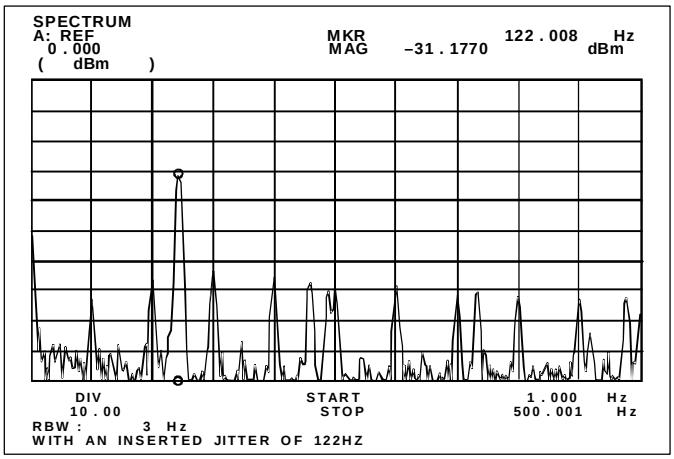
The method uses a clock extractor (see *Appendix A, Section A5.1.*), a phase demodulator and either a spectrum analyzer or an oscilloscope with an FFT display option.

Measurement procedure

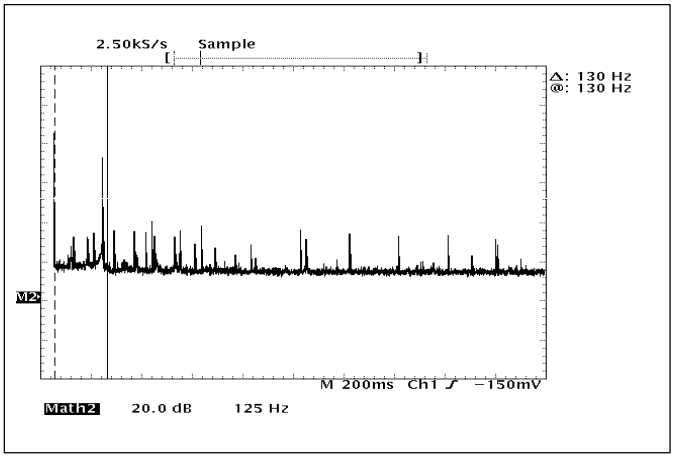
The phase demodulator is fed with outputs 1 and 2 of the clock extractor (as shown in *Appendix A, Fig. A5*).

If the jitter amplitude is greater than 1 UI, the clock divider should be switched into operation (division by the factor *n*).

The output of the phase demodulator (output 3) is displayed using the oscilloscope (FFT display mode) or the spectrum analyzer, giving a display similar to the examples shown in *Fig. 11*. In these examples, a dominant jitter frequency of 122 Hz is apparent.



Spectrum analyzer



FFT display on oscilloscope

Fig. 11 – Examples of jitter spectrum displays obtained using a phase demodulator.

Presentation of results

The dominant jitter frequencies and their amplitudes should be noted in the measurement record, together with the clock recovery bandwidth (*B1* or *B2*), the clock divider setting (*n*) and the resolution of the spectrum analyzer (if used).

Note: The phase demodulator method covers jitter frequencies from 10 Hz to 5 MHz. This range does not include all frequencies up to 27 MHz, as required in the SDI measurement specifications (see *Section 4.2.5.a)*).

4. Measurement of all–frequency jitter with an oscilloscope triggered from a reference signal

Measurement equipment

The method uses an oscilloscope with a bandwidth of 500 MHz. A digital storage oscilloscope with infinite persistence is recommended.

Measurement procedure

The output from the SDI unit under test is fed to the vertical channel of the oscilloscope. The oscilloscope must be triggered directly by a reference clock from the SDI signal source. A trigger signal at 270 or 27 MHz is recommended.

If the jitter amplitude is greater than 1 UI, clock dividers should be inserted in both the SDI signal and the trigger paths, and set for division by the same factor *n* (see *Appendix A, Section A5.1.*).

This method measures all–frequency jitter, which includes frequencies below 10 Hz ("wander"). An example of the display seen on the oscilloscope is given in *Fig. 12*.

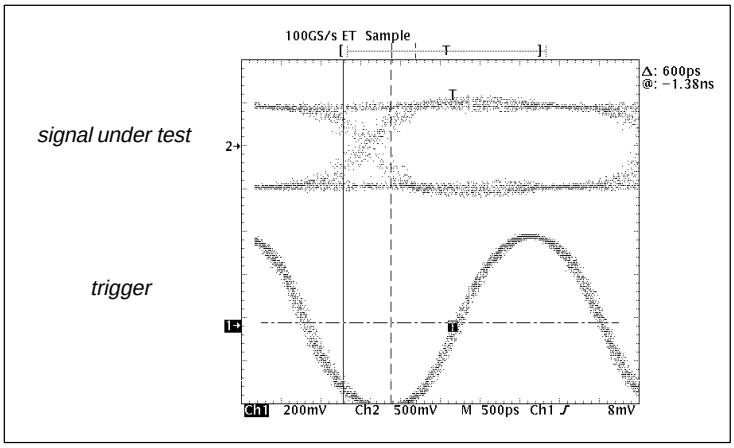


Fig. 12 – Example of all–frequency jitter, displayed on an oscilloscope triggered from a reference signal.

Presentation of results

The measured all–frequency jitter should be noted in the measurement record

Notes: The measurement results will depend significantly on the stability of the reference clock.

If no stable reference clock is available (i.e. the SDI signal only is provided), one of the methods described above using a clock–extractor must be used.

5. Measurement of the jitter spectrum using a spectrum analyzer (jitter frequencies above 27 MHz)

Measurement equipment

The method uses a spectrum analyzer with a bandwidth of 500 MHz and a resolution bandwidth of 10 Hz.

Measurement procedure

The SDI signal is fed directly to the spectrum analyzer input. The centre frequency of the analyzer is set to the third harmonic of the SDI signal (405 MHz). This method ensures that the amplitude ratio between the modulated SDI signal and the jitter frequency is sufficiently large to allow observation of the jitter frequencies.

4.2.6. Return loss

A low value of return loss is more likely to cause problems when short cable lengths are used. With long cable lengths, the effect of a mismatch is reduced owing to the greater cable attenuation.

Specification

The output and input impedance of the serial interface should be 75 Ω. The return loss should be at least 15 dB at all frequencies from 10 to 270 MHz[6].

Measurement equipment

Return loss can be measured with a network analyzer or with a spectrum analyzer, a 75 Ω return loss bridge and a tracking generator.

6. SMPTE Standard 259M [S.6] specifies a frequency range of 5 to 270 MHz.

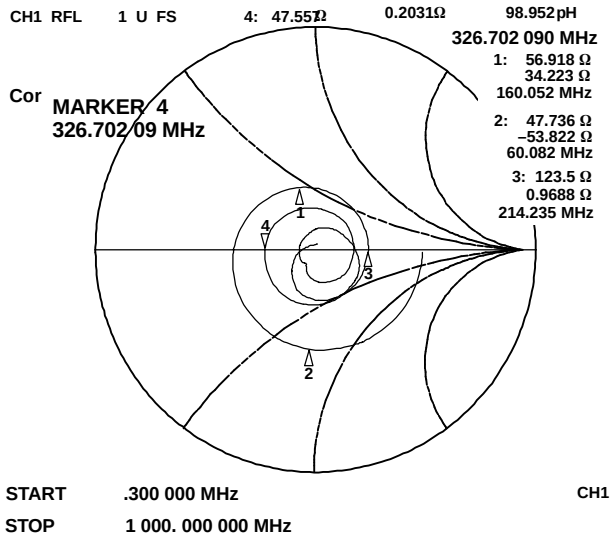
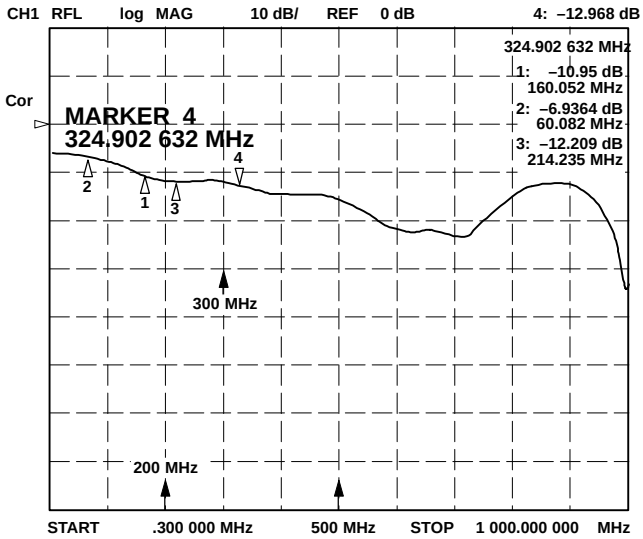


Fig. 13 – Example of the measurement of return loss at the input of SDI equipment.



Measurement conditions and procedure

The equipment under test is set to its normal operational mode and the SDI input and output impedances are measured over the required frequency range.

If a spectrum analyzer is used, the output return loss can only be measured if the output signal is muted; otherwise the signal at the output of the SDI transmitter will interfere with the spectrum analyzer display.

Presentation of results

The worst value of the return loss, in decibels, should be noted in the measurement record, together with the frequency at which that value occurs.

Fig. 13 shows an example of return loss measurements at the input of a typical SDI equipment.

4.2.7. Cross–talk between serial interfaces

The equalizer at the input to an SDI equipment should have a total equalization range of 40 dB at 270 MHz. If there is no wanted signal present at the input, the equalizer will be in its "full gain" position and cross–talk can cause distorted – or almost distortion–free – signals to appear at the output.

To minimize the effects of cross–talk, the greatest attenuation should be at frequencies close to the clock frequency.

Specification

There is no specification for cross–talk.

Measurement equipment

Cross–talk can be measured using a spectrum analyzer with a tracking generator, or a network analyzer with a tracking generator.

Measurement procedure

Considering, as an example, the measurement of cross–talk originating in an SDI switching matrix and affecting an SDI channel, the tracking generator output is fed to all the inputs of the matrix and the cross–talk is measured at the *input* of the SDI channel in question. The tracking generator frequency is swept across the whole frequency range of interest.

Presentation of results

A hard–copy of the spectrum analyzer results showing both the input (test) signal and the cross–talk signal, is used to determine the cross–talk. The cross–talk is given by the following formula:

$$\textit{Cross–talk} = 20\, lg \left(\frac{V_1}{V_2}\right)$$

where: V_1 = input signal amplitude
V_2 = measured signal at input of SDI channel under test.

The worst value of the cross–talk, in decibels, should be noted in the measurement record, together with the frequency range over which measurements were taken.

4.2.8. PLL clock recovery

Measurement equipment

The performance of the clock recovery circuits and the automatic cable equalizer of an SDI receiver is verified using a test–signal generator delivering an SDI check field (see *Section 6.3.2.*), a picture monitor and a BER or EDH analyzer.

Measurement procedure

The output of the SDI receiver is displayed on the picture monitor. Impairments fall into two categories:

– short–duration spots, caused by PLL errors;

– "scratches", of about 50 µs duration, caused by equalizer errors (see *Section 4.2.9.)*.

The receiver output can also be checked with the BER or EDH analyzer.

Presentation of results

The test report should include a record of any impairments noted when using the SDI check field.

Numerical results should be given as the mean time between errors or the bit–error ratio (see *Section 6.4.*).

4.2.9. Cable equalization range of the SDI receiver

Background information on the subject of cable equalization in SDI receivers is given in *Appendix B.*

Specification

EBU document Tech. 3267 [S.3] specifies that the cable equalizer should be able to compensate for up to 40 dB of cable attenuation at 270 MHz. SMPTE Standard 259M [S.6] recommends compensation for 30 dB at one–half of the clock frequency; this corresponds to about 42 dB at 270 MHz, assuming a cable characteristic of $1 \geq)^{-}$.

Measurement equipment

Cable equalization is measured using a test–signal generator providing a colour–bar signal and SDI check field, a bit–error rate (BER) analyzer and a picture monitor. A set of studio cables of different lengths (2, 5, 10, 20, 50, 100 m) and known frequency/attenuation characteristic, or a cable simulator (cable clone), are also required.

Measurement procedure

The colour–bar signal from the test–signal generator is connected to the SDI receiver via different cable lengths, or via the cable clone.

The attenuation of the SDI signal at the equalizer input is varied by increasing the cable length between the generator and the equipment under test. The (equalized) SDI signal at the output is measured with the BER analyzer and verified on the picture monitor.

The procedure should be repeated with the SDI check field.

Presentation of results

The maximum cable length that can be used without affecting the output should be noted in the measurement record.

4.2.10. Dynamic range of SDI receiver input amplifier

Background information concerning the dynamic range of SDI receivers is given in *Appendix B.*

Specification

There is no specification for the dynamic range of the input amplifier of an SDI receiver.

Measurement equipment

The dynamic range is measured using a test–signal generator and a bit–error ratio (BER) analyzer or an oscilloscope with a bandwidth of 500 MHz. The signal generator should be able to deliver either a colour–bar signal and a variable low–frequency (0 to 10 kHz) signal superimposed upon the SDI output, or an SDI check field.

Measurement procedure

The receiver is connected to the generator with a short cable (less than 2 m). If the colour–bar signal is used, the amplitude and frequency of the superimposed low–frequency signal are varied until the first bit–errors occur.

The SDI check field is one of the most critical signals for the serial digital system and will give an approximate overview of the dynamic range performance.

Presentation of results

The maximum amplitude of the superimposed signal that can be applied without causing bit–errors should be noted in the measurement record, together with the frequency corresponding to that amplitude.

4.2.11. Most important measurements in the SDI physical domain

Table 3 lists the most important measurements that should be carried out on all SDI equipment to ensure proper functioning.

Table 3 – Required measurements in the physical domain (SDI).

Measurement	Described in *Section*
Eye pattern	
Signal level	*4.2.2.*
Signal ripple	
Low–frequency signal level distortion	
DC offset	*4.2.2.*
Overshoot	*4.2.4.*
Rise and fall–time	*4.2.3.*
Impedance	*4.2.6.*
Return loss	*4.2.6.*
All–frequency jitter	*4.2.5.*
Weighted jitter (jitter spectrum)	*4.2.5.*
Cable length simulation	*4.2.9.*

Chapter 5

System aspects

Most of the discussion in the previous Chapters has been concerned with individual items of equipment using digital video interfaces, and the serial digital interface (SDI) in particular. In the final analysis, however, the technical quality of programmes made using digital technologies depends not on isolated equipment but on complete production systems. It is important, therefore, to understand how SDI and other digital video and audio equipment performs in a complete, practical studio configuration. Key issues in this field are timing and synchronization, and the physical installation of equipment (cables, connectors, etc.).

5.1. Relative timing between video and audio – General considerations

There are numerous circumstances, such as when televising a large sporting event, when it would not be appropriate for the sound and vision to be time–coincident. Any programme, whether from a studio, an outside broadcast or an editing suite will have a particular timing relationship between the sound and vision and this should be maintained throughout the rest of the broadcast chain.

Methods have been suggested for marking a reference point, which is coincident in the sound and vision signals, to indicate the intended timing relationship in a programme. The marks can be examined at points along the chain including playout, distribution and transmission, and corrections can be made using variable delays if a problem is detected. Various systems are being developed for this purpose.

In cases where a timing mark is not used, or where the production requirement is not known, guidance can be obtained from the following considerations:

– An event in nature is usually observed with the vision occurring before the sound.

– The relative timing of sound to vision should normally lie in the range from sound leading vision by one field, to sound delayed in relation to vision by two fields. These limits correspond to timings of +20 ms to –40 ms for 625–line signals. EBU Technical Recommendation R37 gives limits of +40 to –60 ms [S.23]. Larger differences are noticeable and the subjective impact of the delay depends on the picture and sound content.

One of the differences between analogue and digital systems, apart from the processing principles, is that in a digital system the processing takes a relatively long time. The processing delay in an analogue system may be of the order of a few microseconds, it may be two or three orders of magnitude larger in a digital system.

In video production systems operating in accordance with ITU–R Recommendation BT.601, the maximum synchronizing delay introduced will be 40 ms. Even if the total processing delay for the video signal may be large (several frames), large parts of that delay may be fixed and therefore subject to easy fixed compensation by the provision of a corresponding audio delay. Some of the delay problems caused by frame synchronizers can be eliminated by carrying the audio as an embedded signal in the ancillary data channel of the video signal (see *Section 1.1.5.b)*), since the audio will then be subjected to the same delay as the video; however, some synchronzers will not pass the ancillary data channel.

The best way to compensate for variable video delays is the insertion of audio delays with automatic control.

It should be noted that if bit–rate reduction systems are introduced in the production chain, video/audio timing problems may become more severe. The coding delays in such systems may amount to several hundred milliseconds, for both the video and the audio. So far such techniques have been applied only to the video signal, but if audio delays also become very large it could become necessary also to use compensating video delays.

5.2. Relative timing between video and audio signals in the analogue domain

5.2.1. General

In an analogue environment, the only significant processing delay is that introduced by CCD cameras. The video signal representing an event in the scene may be delayed, in relation to the corresponding audio signal, by a maximum of 20 ms because of the time taken to clock out one field from the sensors. Some of this delay is compensated for by the time it takes sound to travel from the source to the microphone. A distance of approx. 3 m delays the audio by 10 ms. If the processing chains (for both video and audio) are analogue, the delays within the equipment do not need to be taken into account as they are in the order of microseconds.

Further considerations regarding audio/video delays will be found in *Section 5.1*.

5.2.2. Synchronization

When there is the need to synchronize the video signal in an analogue environment a digital synchronizer will have to be used. Depending on the choice of hardware used for this purpose, the delay introduced in the video path can vary within wide limits. If the source is a PAL signal and the synchronizer is an 8–field unit, the delay may vary from below 20 ms to 160 ms. The only efficient and safe way to introduce the necessary delay in the audio path is to use a digital audio delay that automatically tracks the video delay. One practical problem is that there is no standard protocol for the communication between video synchronizers and video delays. For successful operation of the audio delay unit, it must be able to read and react to the delay data provided by the video synchronizer.

5.2.3. The use of digital video effects systems

In an analogue environment, use is often made of digital video effects systems (DVEs). These units usually introduce one full frame (40 ms) of video delay. Since the DVEs can be switched in and out of the video chain from scene to scene, the audio delay should ideally follow. However, it may be unacceptable to switch 40 ms of audio delay in and out of circuit, so audio delays will probably have to be faded in and out.

5.2.4. Cascaded delays

The only good solution to the problem of cascaded delays, is the use of a system that automatically measures and registers the amount of departure from the set timing relationship for any programme. Information obtained using the reference marks on sound and vision signals is used to control compensating audio delay units during playout, distribution or transmission, as necessary.

5.3. Synchronization of an SDI studio

An analogue synchronization signal is specified in EBU Technical Standard N14 [S.21]. The maximum allowable jitter is specified as ± 2.5 ns. However, practical experience has shown that the limit should be < ± 0.5 ns.

The generator for the synchronization of a digital studio should have several outputs having independently–adjustable delay–time settings for black burst video reference and the AES/EBU digital audio reference.

If cascaded reference clock generators are used in an SDI studio, particular attention must be paid to the jitter component which is created by this genlock mode. For further discussion of jitter, see *Section 4.2.5.* and *Appendix A*.

5.3.1. Synchronization of video equipment

Today, most studio equipment has an analogue genlock input even though the jitter stability using a digital synchronization signal is better, if it is derived from a high stable digital source.

Jitter measurements on analogue sync generators have shown that usually the greatest amount of jitter occurs in the vertical–blanking area. The reason for such a behaviour lies in the special PAL structure of the

signal (e.g. 25 Hz offset). Good quality analogue genlock generators should have less than ± 0.5 ns jitter for all frequencies measured over several fields.

To maintain better jitter stability, digital equipment in the studio should be locked to the synchronization signal via the chrominance subcarrier signal and not via the edge of the line synchronization pulse.

The video and audio clocks must be derived from the same source, because frequency differences could eventually result in a missing or additional sample within the audio frame.

5.3.2. Synchronization of audio equipment

The synchronization of digital audio equipment is covered by several reference documents including AES 3 [S.29] and AES 11 [S.41]. The following points should be noted:

The use of an analogue video waveform (black burst) is recommended. A digital equivalent may be used provided the associated A/D or D/A conversion times are taken into account.

If a Digital Audio Reference Signal (DARS) is used, it should conform to the specification given in AES 3. The sample data may represent either silence or an audio signal.

Audio and video reference signals, when used, should be timed as shown in *Ref. 12a).* The tolerance should be ≤ 1 µs.

According to AES 11 the jitter should be within ± 20 ns. (The AES is considering a possible revision of this tolerance to ± 2 ns.)

The digital audio frames must be in phase with the DARS, with a tolerance of ± 5% of an audio frame at a transmitter and ± 25% of an audio frame at the receiver, as shown in *Ref. 12c).*

The frequency stability of the reference signal should be:

1 part per million of the sampling frequency used, for *grade 1* equipment;

10 parts per million, for *grade 2* equipment.

The maximum jitter of the digital audio signal should not exceed ± 20 ns. The clocks of A/D and D/A converters require less than 0.1 ns of jitter, so it is necessary to use a jitter remover.

Some television equipment (particularly video recorders) expect the audio and video to be clock–locked so there will be a known number of audio samples per frame. This is known as isochronous operation. In 625–line systems there are exactly 1920 audio samples per frame. (In 525–line systems there are exactly 8008 audio samples in 5 frames which means there is a non–integer number of audio samples per frame.)

When the various frequencies are derived from a common clock, or the audio samples are derived from a video signal, the phase relationship remains undefined. Sample alignment may be ensured by adding a phase–locking feature to the clock–locked frequency implementation. This is known as synchronous operation.

Two synchronization modes are defined:

a) Isochronous audio synchronization

In systems using isochronous audio synchronization, the sampling rate of the digital audio is such that the number of audio samples occurring within an integer number of video frames is itself an integer number, as shown in the examples in *Table 4*.

Table 4 – Relationship between audio samples and video frames.

Audio sampling rate (kHz)	Audio samples / video frames	
	625–line video (25 frames/s)	525–line video (29.97 frames/s)
48.0	1920 / 1 frame	8008 / 5 frames
44.4	1764 / 1 frame	147147 / 100 frames
32.0	1280 / 1 frame	16016 / 15 frames

Isochronous audio operation is used in situations where exact audio phasing of acquired audio data does not need to be maintained. This includes almost all applications in television today. If multi–channel sound is being carried (or stereo sound with the left and right signals carried by separate AES/EBU digital audio streams) problems may occur as a result of differential delays or different timing instants; this will not be a problem, however, if AES/EBU channel–pairs are used for stereo. Bit–slip is allowed in isochronous operation, and no phasing of the digital audio to a reference, internal or external, is required. The main requirement is an AES/EBU receiver that will buffer the digital inputs and re–establish audio frame alignment to an arbitrary phase while providing some hysterisis to avoid sample phasing jumps. This is a similar requirement in receivers to that for synchronous operation, except that in isochronous operation there is no average phase, leaving the way open for sample bit–slip. Since most television equipment today does not use the digital audio reference signal (DARS) or include a method of phasing the digital audio to the video, isochronous operation is widely used.

It should be noted that synchronization is maintained when switching is done in a mixer but not when it is done in a matrix. The reframer detects the absence of correct synchronization and inserts frames of silence until the PLL locks up again. The problem shows up as clicks and pops on the audible signal which have to be removed in down–stream processing.

b) Synchronous audio synchronization

In systems using synchronous audio synchronization, the phase of the audio samples has a defined relationship to other audio samples and the associated video. In other words the audio is isochronous and has a defined phase.

Synchronous audio operation is required in cases where the exact phasing of acquired audio data must be maintained throughout the system. An example would be the requirement to produce an exact audio image position. In synchronous audio operation no bit–slip is allowed.

All analogue audio signals that are to maintain channel–to–channel timing shall be sampled with nominally identical 48 kHz clock phases locked to the video signal. The X or Z preamble of the AES/EBU audio frames must meet the data sample timing tolerance, $T = \pm 1.0$ µs, at the source as shown in *Ref. 12a)*.

Where an AES/EBU audio signal is reconstituted after processing, the relative sample timing must be reproduced. Examples of a reconstituted source would be the output of one or more digital tape recorders, or several embedded audio demultiplexers. The delay for each channel must be repeatable, time–invariant and machine–independent. This can be accomplished, in part, by locking the audio sample phase at each output to a common time position in the audio frame sequence.

Embedded audio systems require the use of buffers in both multiplexing and demultiplexing equipment. In order to maintain channel–to–channel timing the delay through each function in the system must be the same constant value for each channel [13].

5.3.3. External synchronization capability of a digital studio

In principle, a digital outside–broadcast unit or studio should not be synchronized from an analogue outside–broadcast unit. At the present time older clock generators from the analogue studio have a large jitter component, and all signals in the digital studio would then be affected. It is recommended that all input analogue signals are passed through a signal converter (PAL to SDI) with a frame–store synchronization facility.

5.4. Decoding and re–encoding of PAL signals

Signals originated in PAL and subsequently decoded and passed through an SDI studio may suffer from a 6.25 Hz luminance flicker when the PAL signal is encoded at the studio output and subsequently decoded in the receiver.

There are two reasons for this effect:

5.4.1. Cross–effects in the PAL demodulator

The PAL demodulator at the input to the SDI studio demodulates part of the luminance as chrominance and vice versa. When the SDI studio output is re–encoded into PAL, these cross–frequencies will be modulated as “normal” luminance or chrominance respectively. Finally, after demodulation in the home receiver, a 6.25 Hz flicker can be seen. The mechanism can be understood by considering the subcarrier–to–line sync phase, Sc/H:

Sc–H = 25 Hz plus 270° per line; this will generate a 6.25 Hz product in the output of the first demodulator;

Sc–H = 25 Hz plus 270° per line; this will generate a 6.25 Hz product in the modulated signal from the PAL coder at the output of the SDI studio.

The two steps above normally cancel the effect out, so after one PAL encoder/decoder cascade there will be no 6.25 Hz flicker. The final demodulation process in the home receiver will produce a similar effect which is not cancelled:

Sc–H = 25 Hz plus 270° per line; this will produce a 6.25 Hz flicker.

5.4.2. Inaccurate generation of the 25 Hz offset

Differences in generating the 25 Hz offset in the original PAL encoder and the PAL encoder at the output of the SDI studio, can cause a 6.25 Hz flicker. When the 25 Hz offset in a PAL encoder is generated, it is assumed that the 25 Hz modulation of the subcarrier is done following a strict sine function. However, this is not the case in practical PAL encoders, and consequently the relationship between the subcarrier and the line frequency is not stable. There will be a timing difference between subcarrier and line sync, especially in the case of PAL decoders operating with multiples of the sampling frequency, f_{sc} .

Differences between the 25 Hz PLL loop jitter of the source PAL encoder and the PAL encoder at the output of the SDI studio can also lead to a 6.25 Hz flicker.

6.25 Hz flicker effects can be tested with a zone plate or frequency burst test picture.

For further considerations of flicker see *Section 5.7.*

5.5. Cascaded PLLs (reclocking)

If PLLs are cascaded the jitter will increase, but in practical situations this will not cause problems. The number of PLLs that can be satisfactorily cascaded depends on the jitter transfer function and the alignment of each device. Increased jitter amplitudes can occur if the SDI receivers are all of the same design, in which case the jitter transfer functions of the cascaded receivers exhibit small jitter increments at the same point in the jitter transfer function. However in a digital studio equipment of a variety of different types, and from different suppliers will normally be in use so the risk of problems is small.

The run–in time of a SDI receiver is typically about 200 ns. If several PLLs are connected in series, then the overall run–in time will be probably smaller than the sum of the individual run–in times. For example, when the second PLL runs in, it will try to pull–in the third PLL during the run–in phase etc.

For further consideration of jitter and run–in see *Section 4.2.5.* and *Appendix A*, and *Section 2.2.4.*

5.6. SDI to PAL (D_{ser}/A) converters

Various types of PAL converter are used in a digital studio. These converters normally generate create a PAL signal from the serial digital signal and the external reference (black burst).

The SDI signal delivered to these converters is to a greater or lesser degree affected by jitter. This jitter, which can be several nanoseconds, does not cause any problems in the digital domain provided that the jitter frequency is low (see *Section 4.2.5.*). However, problems can arise in the D/A conversion process and also when generating the PAL signal.

Jitter in the SDI signal causes non–linearity in the D/A converter. For this reason any jitter before the D/A converter should not exceed 1 ns.

Jitter also leads to PAL vector and line–sync jitter.

To reduce the phase jitter of the PAL signal, some encoders extract the line sync reference from the digital signal and the subcarrier from the genlock signal. In other words, the subcarrier phase remains correct but the Sc/H phase of the output signal fluctuates with the same rhythm as the jitter of the serial signal.

SDI to PAL encoders can be classified in 3 groups:

5.6.1. Precision PAL encoders for transmission (continuity) output

The encoder used to feed the studio or production centre output to the transmitter network requires an integrated input buffer or, better, a line or frame synchronizer which can eliminate phase jitter on the SDI signal. The synchronizer will add a delay at this point, and consideration should be given to this.

In addition, a gamut limiter is required before (or in) the encoder because the generated PAL signal may be distorted (see *Section 2.2.7.*).

The encoder requires a black burst signal as reference, and it should be possible to blank out single lines in the normally transparent vertical–blanking area.

A jitter remover should be used (see *Section 4.2.5.* and *Appendix A).*

5.6.2. Wideband PAL encoder (C_B, C_R = 2.5 MHz)

In a mixed analogue/digital studio complex, such as can generally be found in most production centres, it may be necessary to have a wideband PAL output.

The signals of the encoder can be decoded with a precision comb filter and transferred back to the levels specified in EBU Technical Standard N10 [S.20] without unacceptable loss. These signals are not suitable for transmission but can be used without problems within the studio.

The encoder requires a black burst signal as reference, and it should be possible to blank out single lines in the normally transparent vertical–blanking area.

A jitter remover should be used (see *Section 4.2.5.* and *Appendix A).*

5.6.3. Low–cost PAL encoders

Coders for monitoring generally use inexpensive filters and operate without genlock. Their internal PAL synchronization is derived directly from the incoming SDI signal. Therefore the incoming SDI jitter is directly transferred to the subcarrier phase and the line sync phase of the output PAL signal.

The four–frame sequence is inherently deficient because this information is missing from the SDI signal. A monitor can operate without problems with these signals.

5.7. PAL to SDI (A/D_{ser}) converters

In a digital studio the input PAL signals are converted into SDI signals. The PAL to SDI converter should have an integrated frame–store synchronizer so that the external source can be synchronized to the studio.

The lines during the vertical blanking should be passed transparently.

Depending on the type of decoding the delay can be up to 40 ms.

At present, the PAL 8–field information is not carried through the SDI interface. Therefore to avoid flicker and other effects in the PAL output signal of the SDI studio the suppression of the subcarrier frequency in the component signals should be better than 46 dB.

The picture to sync position should be exact.

5.8. Thermal considerations for digital equipment

Digital equipment is very compact because of EMC requirements and requires forced ventilation. Failure of the ventilation fan usually leads to equipment failure.

Some manufacturers provide an alarm output in the digital equipment which provides information about the thermal conditions and other parameters. Central temperature monitoring should be included in SDI studio installations.

The SMPTE is currently standardizing fault reporting schemes [S.40][S.38].

5.9. 75 / 50 Ω connectors for SDI

Specifications

Although EBU document Tech. 3267 recommends connectors with an impedance of 75 Ω for the transmission of serial digital signals, most equipment is still fitted with 50 Ω BNC connectors because these are more robust.

A signal that goes through the 50 Ω section reaches 96% of its final value immediately, and 99% after twice the electrical length of the 50 Ω cable. This causes only a small amount of distortion. At the source end of the 50 Ω line, however, there is a 20% reflection that propagates back through the line towards the transmitter. This reflected pulse leads to a reduced eye opening.

If it is assumed that the 50 Ω input socket is 2 cm long, this corresponds to a propagation delay time of approximately 100 ps and the delay of the reflected signal is therefore 200 ps. The effect of this delay can be considered negligible compared with the 1 ns rise–time of the serial signal [2].

Robust 50 Ω sockets are available on the market, equipment manufacturers should be persuaded to fit them.

The mixed use of gold and nickel–coated BNC connectors does not lead to problems.

The connectors should be galvanically connected to the chassis of the equipment.

5.10. SDI cables

Cable with copper braiding and foil shielding should be used for SDI cabling to reduce the emission of SDI signal frequencies, and enhance system immunity from external fields [8].

5.11. Passive loop–throughs and 75 Ω terminations

Passive loop–throughs are possible and practical in certain test equipment.

It should be noted that a “loop through” output is not designed to drive the full cable length of an SDI link.

Special care must be taken when a passive loop–through is not being used. It is important to make sure the termination is 75 Ω, with no significant reactive component at frequencies at least as high as the SDI clock frequency. So–called “precision” terminators of the type commonly used with PAL equipment do not meet this requirement.

5.12. Integration of measurement equipment in a digital studio

In analogue studios, measurement equipment is connected into the system via a video switching matrix and/or an analogue distribution amplifier. Measurement equipment in digital studios, in contrast, must be able to examine the physical signal quality without modifying signal characteristics such as recovery or equalization. Therefore it must be possible to connect the equipment directly to the source via a patch panel without any equalization or reclocking circuit.

Chapter 6

Test and measurement equipment

The incorporation of digital video technology into television production facilities will give many users their first “hands on” experience with a wide range of new equipment, new signal formats, new problems – and new test methods. As in all areas of the electronic media, test and measurement instruments are an essential aid to the testing of systems and the diagnosis of problems.

This Chapter sets out the specialized requirements of test equipment adapted to the SDI environment of the modern television studio.

6.1. Test signal generators

In all signal environments, test signal generators are used to inject signals having known characteristics into an equipment or a system under test, and an analyzer is then used at the equipment output to evaluate the distortions, errors or other unwanted effects.

Test signal generators for use in digital television studios should have several outputs:

– serial digital video (SDI);
– analogue component video;
– parallel and serial clocks (27 MHz and 270 MHz);
– digital audio (optional).

All video test signals should be generated with 10–bit resolution, and they should be delivered to the digital and analogue video outputs simultaneously.

6.1.1. Video and ancillary data

Video and ancillary data test signals should include the following:

– All test signals described in ITU–R Recommendation BT.801 [S.33] (see also *Section 6.3.1.* below).
– All known pathological test signals (e.g. the SDI check field described in *Section 6.3.2.).*
– Colour gamut test signals.
– Signals containing incorrect timing reference signals (TRS).
– Picture position test signal shown in *Fig. 2.*
– Test signals for ancillary data (including embedded audio).
– The video delay time test signal shown in *Fig. 4.*

Other requirements include the following:

– The video level should be adjustable.
– It should be possible to insert test signals into the vertical–blanking interval, in order to test for equipment transparency in this area.

– Generation of relevant ancillary data, including wide–screen signalling (WSS) in line 23 [S.19], should be available as an option.

– For stationary test patterns, error data handling (EDH) information should be delivered so that EDH evaluations can be made. The flags should be switchable to allow tests to be carried out on the downstream equipment ("error received", etc.).

– The generator should be able to read in special test signals, for example from a digital video recorder, and store them for later use.

6.1.2. SDI output

The following requirements concern the SDI output of the test signal generator

– It should be possible to add noise to the SDI output.

– There should be provision for cable stress tests (i.e. simulated insertion of calibrated cable lengths).

– It should be possible to add jitter, in calibrated steps of amplitude and frequency.

– The output level of the SDI signal should be variable, to permit tests of the overload sensitivity of SDI receiver PLLs (see *Section 4.2.2.*).

– The generator should be able to supply several synchronization signals to a studio, each having a different timing. The delay times of each signal should variable over a wide range (4 frames).

6.1.3. Analogue output

The analogue output of the generator should satisfy the following requirements

– It should be possible to add jitter, in calibrated steps of amplitude and frequency.

– The generator should be able to supply several synchronization signals to a studio, each having a different timing. The delay times of each signal should variable over a wide range (4 frames).

6.1.4. Audio output

The generator is required to deliver the standard forms of digital audio reference and test signals, as defined in the relevant AES documentation [S.42].

6.2. SDI analyzer

An SDI analyzer is required to evaluate signal quality in both the physical domain and in the data domain.

6.2.1. Measurements in the physical domain

Measurement methods relevant to the physical domain of the SDI are described in *Section 4.2.* In summary, the following parameters need to be measured:

– Eye pattern

– Signal level

– Signal ripple

– Low–frequency signal level distortion

– DC offset

– Overshoot

– Rise and fall times

– Impedance

– Return loss

– Jitter.

Measurements in the data domain are described in *Chapter 3*. They cover the following aspects:

- Number of active bits (eight or ten)
- Digital signal level
- Check for forbidden digital values
- Timing reference signal (TRS) verification
- Rise and fall times
- Bit–error ratio
- Cyclic redundancy check (CRC)
- Luminance/chrominance delay
- Picture position relative to the TRS
- Ancillary data verification (including type and length identification)
- Colour gamut verification
- Propagation delay in SDI equipment.

6.3. Test signals for the SDI

6.3.1. General test signals

ITU–R Recommendation BT.801 [S.33] describes standard test signals for measurements on the SDI. At present, these signals are all defined using 8–bit video data words, although for some real tests 10–bit signals are required.

6.3.2. SDI check field

a) SDI check field description

The SDI check field is a full–field test signal specifically designed for use with the SDI. It is specified in SMPTE Recommended Practice RP 178 [S.35].

The data–stream of the test signal contains particular sequences of logic “1”s and “0”s which serve to “stress” the transmission system as a means of detecting weaknesses in the system at an early stage. Although the SDI check field stresses the equipment or installation under test, it is not a true “pathological” test signal, in the sense the bit sequences it contains are not forbidden; they could arise in normal operation, even if only rarely.

The SDI check field has two special data combinations, each having a particular purpose:

- one combination checks the performance of the PLL clock–recovery of the SDI receiver, as described in *Section 4.2.8.*;
- the other combination checks the performance of the cable equalizer, as described in *Section 4.2.9.*.

The two data combinations are usually included in the same test pattern, each occupying one half of the picture as discussed in *Section 6.3.1.b)*.

b) SDI check field principles

Considering first the performance of a PLL clock recovery circuit, it is possible that a large number of “1”s may be needed in the video data signal in order to generate the clock with high time precision.

These “1”s are represented in the channel code using the NRZI format as polarity changes (edges), while the “0”s are represented by the absence of transitions (note: NRZI is not a DC–free code). If there are many consecutive “0”s, the clock recovery may be impaired; in effect the PLL oscillator will run “free” for excessively long periods because it has nothing to lock–on to.

The scrambling applied to the data–stream is designed to reduce the number of consecutive “0”s. The nine–bit scrambler (function G1 = x9 + $\oplus$ x4 $\oplus$ 1) can nevertheless generate an infinitely–long sequence of “0”s if the input signal consists only of “0”s. It is therefore necessary to take care, while coding the signal, that this situation never arises whilst, at the same time, ensuring that a code sequence corresponding to the timing reference signal (TRS) never occurs in the active frame.

The longest sequence of “0”s in the active video signal will occur if the value 80.0_{hex} is followed by $01.X_{hex}$, as shown in *Fig. 14*. This combination gives 16 consecutive “0”s.

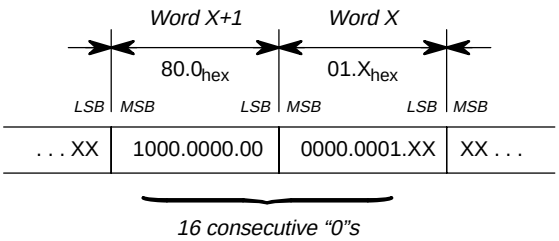


Fig. 14 – Creation of the longest possible sequence of “0”s in active video data words.

As a result of the defined 0 groups, longer sequences of “0”s can appear in the timing reference signal (TRS) area. The TRS for 4:2:2 digital component video signals is $FF.C/00.0/00.0/XYZ_{hex}$ (see *Ref. 6*). This always contains a sequence of 20 consecutive “0”s, and will have 29 if XYZ = 200_{hex}. In the case of a digital PAL signal sampled at $4f_{sc}$, the TRS in the SDI is $FF.C/00.0/00.0/00.0_{hex}$ which contains 30 consecutive “0”s.

If these signals are sent through the NRZ scrambler, the number of “0”s will be increased by nine (the number of levels on the scrambler), and the inversion associated with the NRZI converter adds one more “0”. Consequently, the largest possible number of “0”s is 39 for 4:2:2 digital component signals, extending over a period of 144 ns (40 “0”s for digital PAL, corresponding to a period of approximately 225 ns).

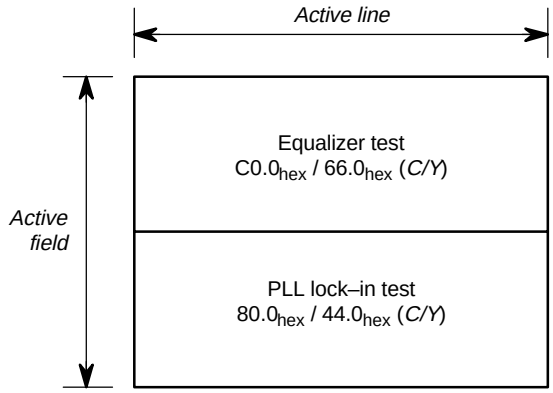
The test signals developed for practical use have a smaller number of “0”s in the sequence. Two sequences have been proposed, one for tests on the decoder PLL and the other for cable equalization, as discussed in *Section 6.3.2.a)*. The equalizer test signal (top half of SDI check field – see *Fig. 15a)*) has the code values $C0.0_{hex}/66.0_{hex}$ (*C/Y*), and the PLL test signal (bottom half of field) has the code values $80.0_{hex}/44.0_{hex}$ (*C/Y*). With the order of luminance and chrominance samples shown in this figure, the top half of the picture will be a shade of purple and the bottom half a shade of grey [1].

Fig. 15b) shows the PLL test signal, with a sequence of 19 “0”s separated by a single “1” which, after the x $\oplus$ 1 inversion produces continuous stream of polarity changes every 20 bits (74 ns). The PLL does not have time–interval phase control and the DC content of this test signal is close to zero.

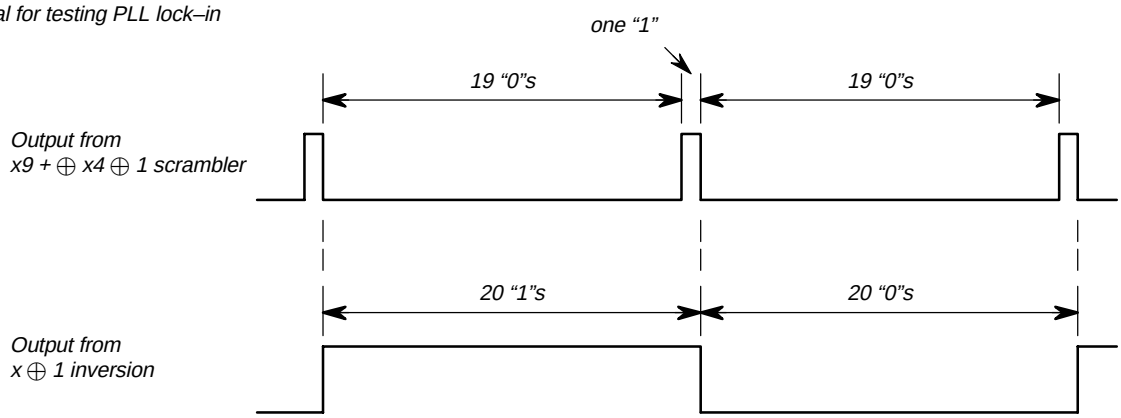
Fig. 15c) shows the equalizer test signal, as it appears before and after the x $\oplus$ 1 inversion. It comprises 19 periods of a low level followed by a single period at high level. The mean DC level is no longer zero, owing to the 3.7 ns interruption every 70.3 ns. If there is a fault in the equalizer, the mean level will change, in a manner similar to a clamping error. The receiver equalizer takes the peak–to–peak values of the signal as a reference so, depending on the time–constant, rapid regulation events can occur if a long sequence of “0”s is transmitted.

Table 5 shows typical distributions of sequences of “1”s and “0”s in a 100–frame period of component black. *Table 6* shows similar data for 100 frames of the SDI check field. The sequences of 19 and 20 consecutive “0”s are responsible for the low–frequency stressing of the system. When they occur (about once per frame), they occur for a full active television live and cause a significant low–frequency disturbance. The PLL test signal is a 20–“1”, 20–“0” square–wave, so there is an even number of each type of sequence. The equalizer test signal has sequences of 19 “1”s followed by a “0”, or 19 “0”s followed by a “1”; an additional “1” in each frame forces the two polarities to occur and both are represented in the data [5].

(a) *SDI check field, as displayed on a picture monitor*



(b) *Signal for testing PLL lock–in*



(c) *Signal for testing cable equalization*

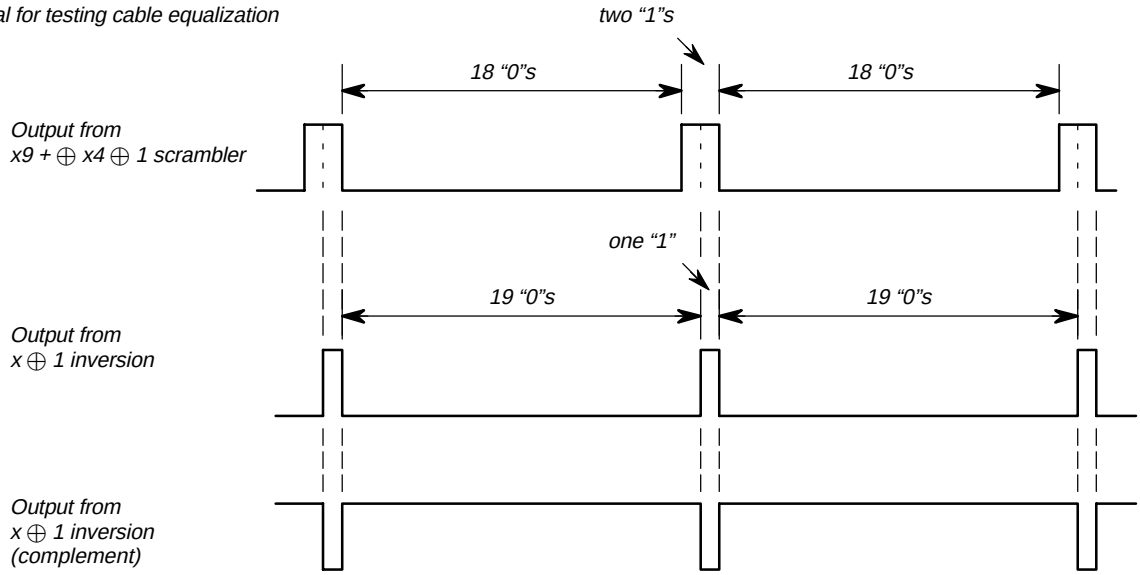


Fig. 15 – Composition of the SDI check field.

Table 5 – Lengths of sequences of “0”s and “1”s in 100 frames of component black.

Length	“1”s	“0”s	Length	“1”s	“0”s
1	112615438	112610564	21		13579
2	56303576	56305219	22	73759	
3	28155012	28154963	23		
4	14076558	14077338	24		
5	7037923	7038595	25		
6	3518756	3518899	26		
7	1759428	1760240	27		
8	1059392	699666	28		
9	610241	970950	29		
10	1169	1060	30		
11	14	156	31		
12	40		32	55	51
13	156	114	33	49	
14			34		3
15			35		
16	13713	73865	36		
17			37		
18			38		
19	101	94	39		50
20			40		

Table 6 – Lengths of sequences of “0”s and “1”s in 100 frames of the SDI check field.

Length	“1”s	“0”s	Length	“1”s	“0”s
1	112595598	112595271	21		
2	56291947	56292583	22	9344	9425
3	28146431	28147229	23		
4	14073813	14072656	24		
5	7035240	7035841	25		
6	3518502	3518856	26		
7	1758583	1758969	27		
8	879203	879359	28		
9	706058	706029	29		
10	51596	51598	30		
11	146	154	31		
12	16858	16817	32	49	49
13	34405	34374	33	35	32
14	17445	17442	34	3	4
15			35		
16	9558	9588	36		
17			37		
18	29	27	38		
19	20944	19503	39	13	14
20	19413	19413	40		

6.4. Bit–error ratio (BER) measurements

6.4.1. Significance of BER values

The bit–error ratio (BER) is the ratio of the number of incorrect bits received to the total number of bits received. As an example, consider the serial digital interface (SDI) which has a data–rate of 270 Mbit/s. If there were one error per frame, the BER would be:

$$BER = \frac{25}{(270 \times 10^6)} = 0.93 \times 10^{-7} \quad \text{for 625–line systems}$$

or:

$$BER = \frac{30}{(270 \times 10^6)} = 1.11 \times 10^{-7} \quad \text{for 525–line systems}$$

To illustrate the significance of BER values, *Table 7* relates mean time intervals between errors to approximate BER values in the case of the SDI.

Table 7 – BER values for selected mean times between errors in the SDI.

Mean time between errors	BER in SDI at 270 Mbit/s
1 television frame	1×10^{-7}
1 second	4×10^{-9}
1 minute	6×10^{-11}
1 hour	1×10^{-12}
1 day	4×10^{-14}
1 week	6×10^{-15}
1 month	1×10^{-15}
1 year	1×10^{-16}
1 decade	1×10^{-17}
1 century	1×10^{-18}

The BER is a useful measure of system performance in situations where the signal–to–noise ratio at the receiver is at such a level that random errors occur.

Scrambling is used in the SDI to reduce the DC component of the transmitted signal and ensure that the signal reaching the receiver has a sufficiently large number of zero–crossings to permit reliable clock recovery. It is an inherent feature of the descrambler that a single bit error will, in every case, cause an error in two data words (samples). Also, there will be a 50% probability that the error in one of the words will be in either the most–significant bit or in the second–most significant bit. Therefore, an error–rate of 1 error per frame will be noticeable by a reasonably patient observer. The fact that the error is noticeable is sufficient to make it unacceptable (in purist engineering terms, at least, if not subjectively), but it is even more unacceptable because of the indications it gives about the operation of the SDI system.

6.4.2. Measurement of BER

BER measurements can be made directly using equipment designed for this purpose. Unfortunately, in a properly–operating system with, for example, 6 dB of headroom (corresponding to the attenuation of about 80 m of cable), there will be no errors to measure and the result will be a BER of zero. This is because the SDI system normally operates in an environment which is free from random errors. If errors are never going to occur, as implied by *Table 7*, there will be nothing to measure. A more common problem in practical installations will be burst errors due to an interfering signal such as a noise spike which occurs intermittently and very infrequently. Another possible cause might be cross–talk that may come and go depending on signals being used at any particular time. A poor electrical contact at an interface might cause noise only when it is mechanically disturbed.

Owing to the intermittent nature of burst errors, data recording and communications engineers have defined another error–measurement concept, called the “errored second”. The advantages of this concept can be illustrated by an example:

Suppose that a burst error causes 10,000 errors in two frames of video. A BER measurement over a period of one minute would indicate a BER of 1×10^{-6}, and a measurement over a full day would indicate 8×10^{-9}. In contrast, an “errored second” measurement would indicate that there was one second containing errors and that it occurred 3 hours, 10 minutes and 5 seconds ago. The “errored second” concept is clearly a more useful measurement method in this case.

A significant advantage of the “errored second” as compared to a conventional BER measurement is that it gives a better indication of the fitness for service of links that are subject to burst errors. The SDI is in this category of system because television images are greatly disturbed by momentary loss of synchronization. A BER measurement could give the same value for a single, large error burst as it would for several shorter, scattered bursts; however, if each of those shorter bursts causes momentary loss of synchronization the subjective effect would be more damage to the viewed picture than that caused by the single. longer burst. It is therefore proposed that the “errored second” concept (and the inverse concept of “error–free seconds”) should be used for digital television signals [3].

6.5. Electronic data handling (EDH)

System measurements using techniques such as the SDI check–field are “invasive” in the sense that they require the transmission of a special test signal. Such tests can therefore be done outside normal production hours only. As a response to the need for continual SDI monitoring during normal programme–making operations, the electronic data handling (EDH) system has been developed [S.39]. EDH data are calculated using the programme signal as a test signal, and embedded as ancillary data in lines 5 and 318.

The EDH system calculates two CRC check–words for each digital field:

– one calculated over the active picture area (excluding lines corresponding to half–lines in the associated analogue systems);
– the other calculated over a full field of the video signal (except the lines 5 and 318 which carry the EDH data itself, and the two following lines where video switching and subsequent framing verification occur).

EDH also includes flags to indicate whether a detected error has been passed on from up–stream equipment or has occured in the equipment in which the EDH checking is currently being carried out.

By observing the EDH indications from different items of equipment in a chain, an item which is causing errors can be isolated and a verification of the check–sums can assist in localising the fault within that equipment. It should be noted that errors flagged by an item of equipment refer to the *previous* field.

Reference data and Standards

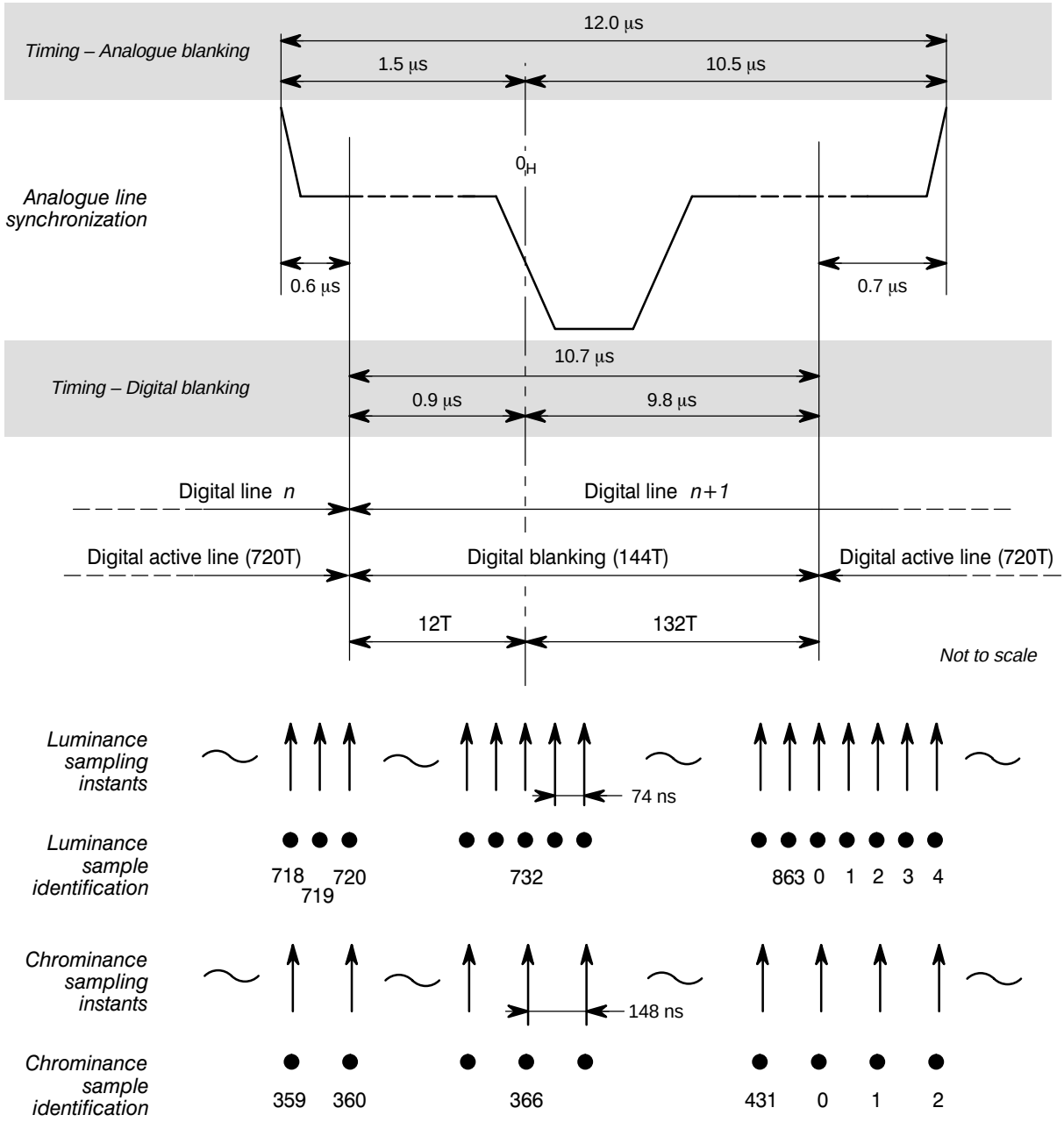
The interfaces discussed in this document are complex and flexible assemblies of sub–systems whose specifications and standards are distributed among a large number of reference documents. This *Reference data and Standards* section groups together the essential information needed in the framework of measurements on interface equipment and systems.

Except where otherwise indicated, all reference data considers the case of 625–line 50 field/s television systems only.

Reference data

This Section reproduces the principal reference data for the digital component video interfaces.

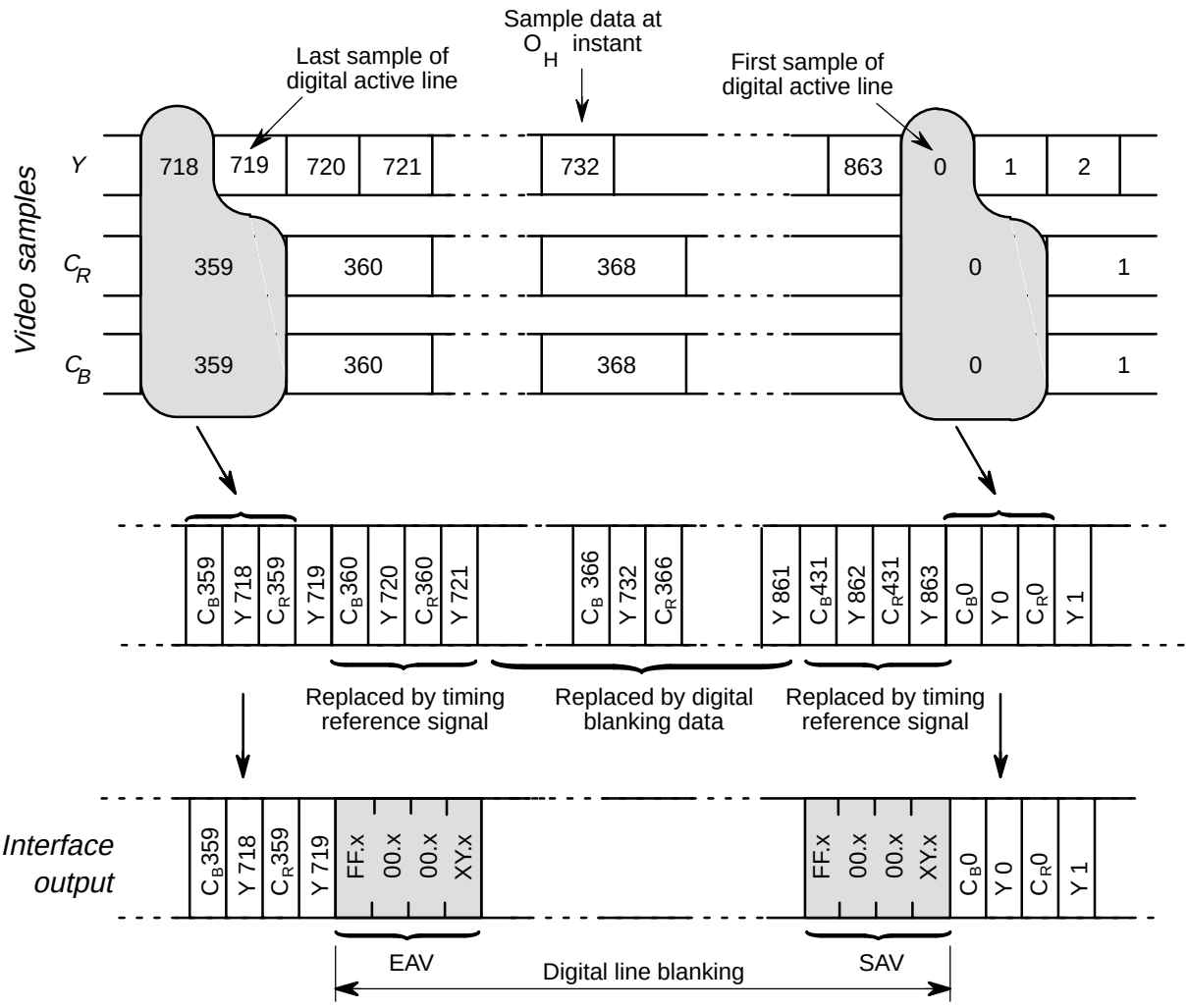
The diagrams and tables have been taken from the relevant standards documents and adapted where appropriate for the purposes of the present document. They may therefore contain additional information which does not constitute part of the formal standards.



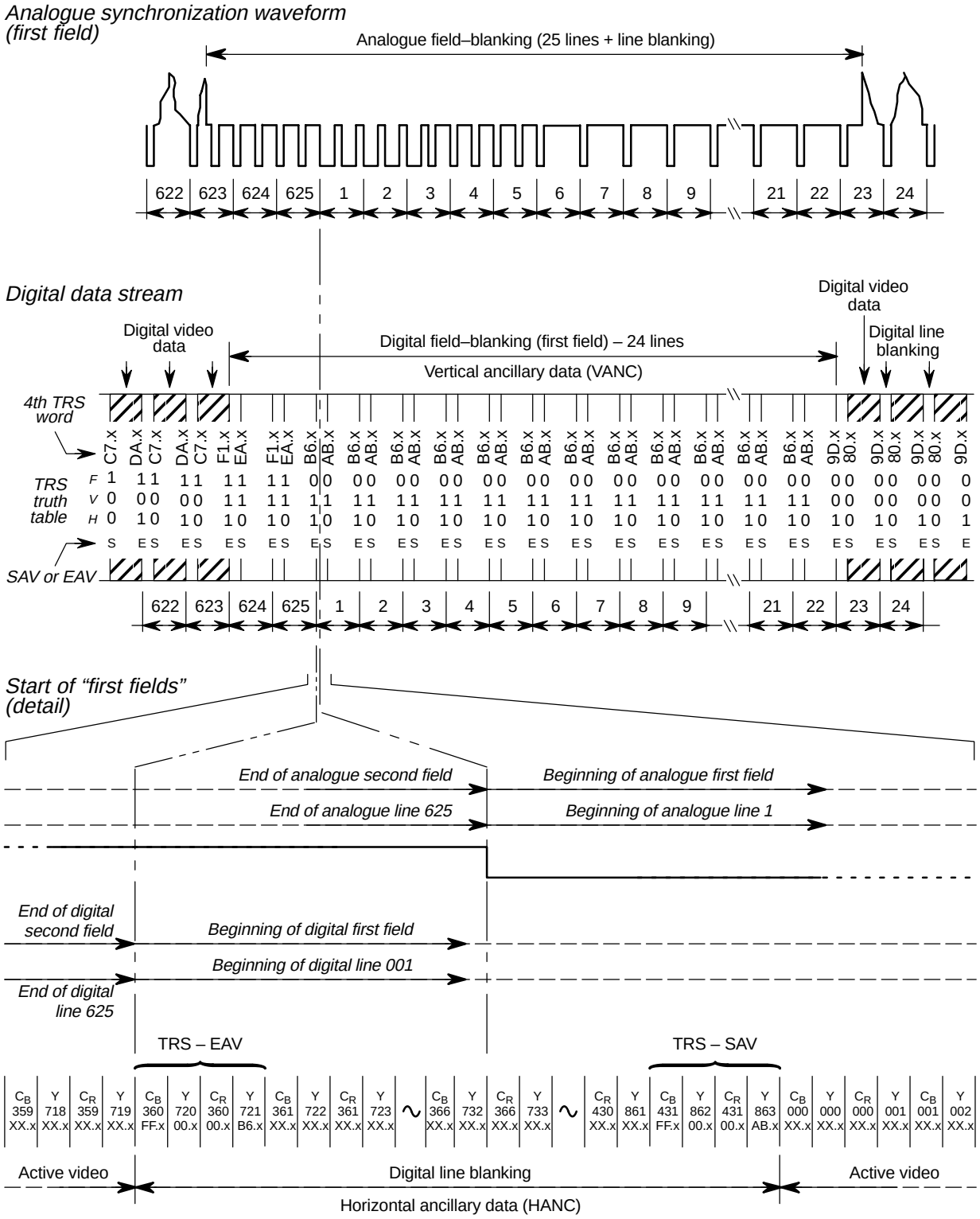
Notes:

1. Digital blanking contains 144 luminance samples, numbered 720 to 863, and 72 chrominance samples, numbered 360 to 431 in the figure. The digital active line contains 720 luminance samples, numbered 0 to 719, and 360 chrominance samples, numbered 0 to 359 in the figure.
2. The position of digital blanking shown in the figure was chosen so that the digital active line is symmetrically disposed in relation to the permitted variations, specified relative to the line synchronization reference O_H, in the start and finish times of the analogue active line.
3. For identification purposes, word “0” is taken as being the first word of the digital active line.
4. 0_H is the analogue line timing reference, set at the mid−amplitude point of the leading edge of the analogue line synchronizing pulse.
5. T is the sampling period (10^3/13.5 ns)

Ref. 1 – Correspondence between the digital and analogue blanking intervals, and the analogue line synchronization.



Ref. 2 – Composition of the data multiplex and position of the timing reference signals, EAV and SAV.

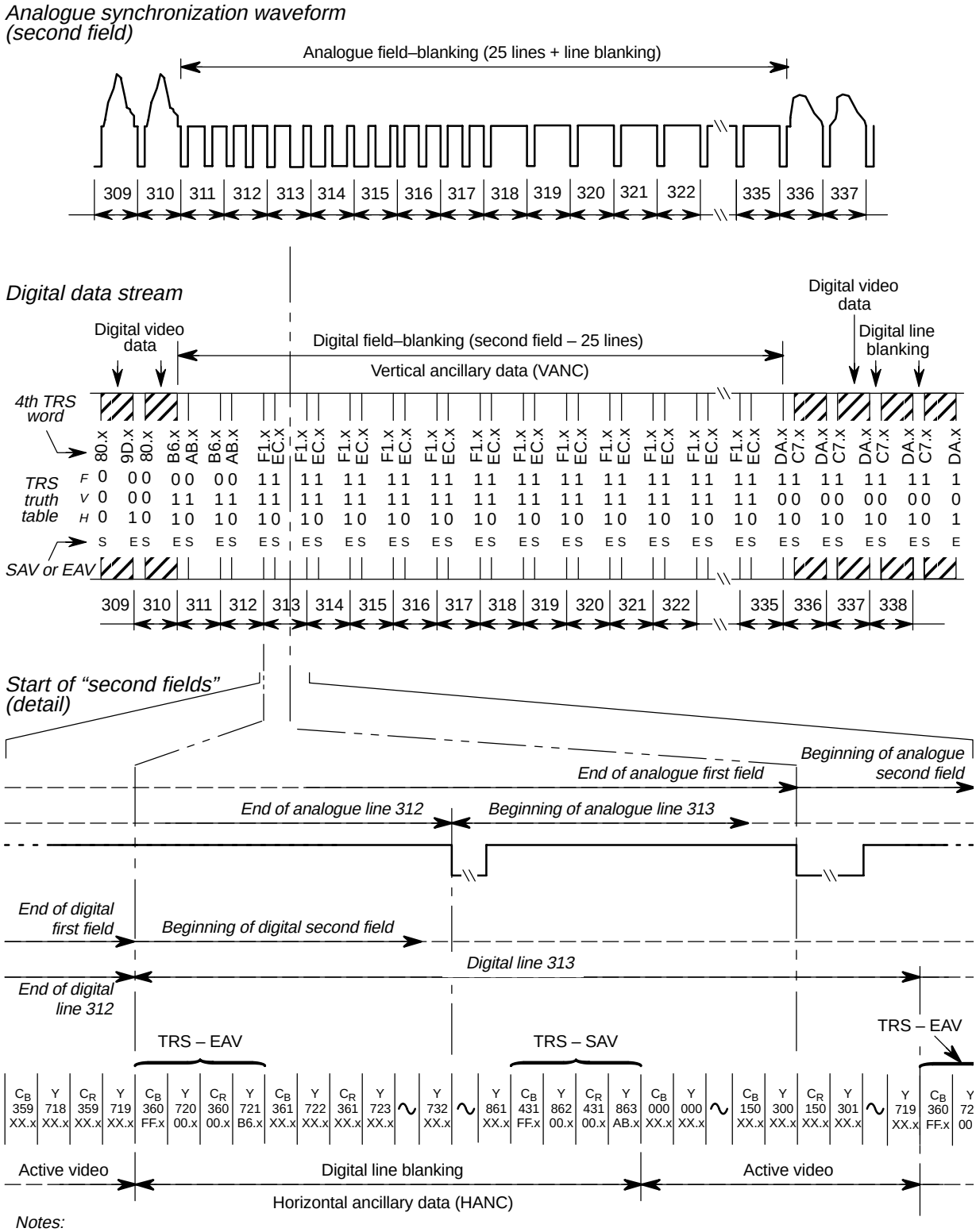


Notes:

1. The allocation of active lines in the digital fields was arranged in such a way as to avoid the digital processing of half–lines. The number of active video lines is 288 in both fields, and the width of digital field–blanking is 24 lines preceding the active part of the first field and 25 lines preceding that of the second.

2 Blanking appropriate to the national broadcasting standard should be applied at the point at which the signal is converted to the analogue form.

Ref. 3a) – Relationship between the digital and analogue fields, showing also the position of the digital field–blanking interval – first field.

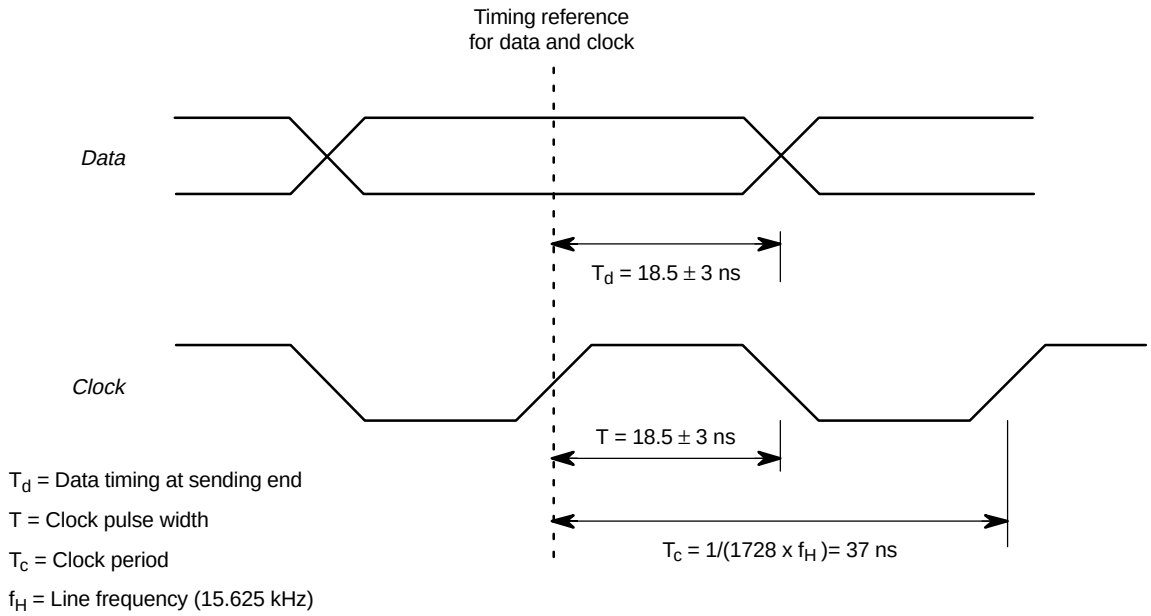


Notes:

1. The allocation of active lines in the digital fields was arranged in such a way as to avoid the digital processing of half–lines. The number of active video lines is 288 in both fields, and the width of digital field–blanking is 24 lines preceding the active part of the first field and 25 lines preceding that of the second.

2 Blanking appropriate to the national broadcasting standard should be applied at the point at which the signal is converted to the analogue form.

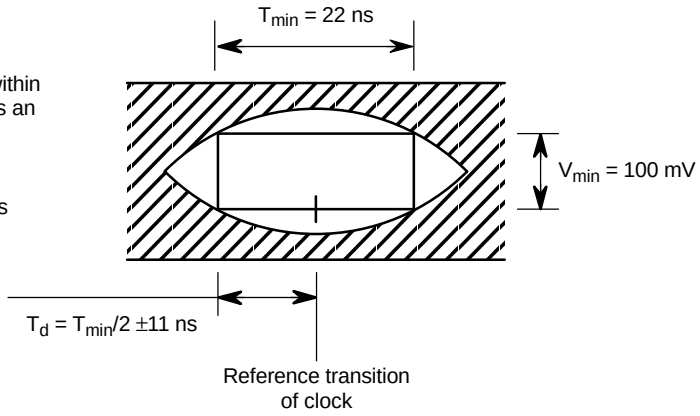
Ref. 3b) – Relationship between the digital and analogue fields, showing also the position of the digital field–blanking interval – second field.



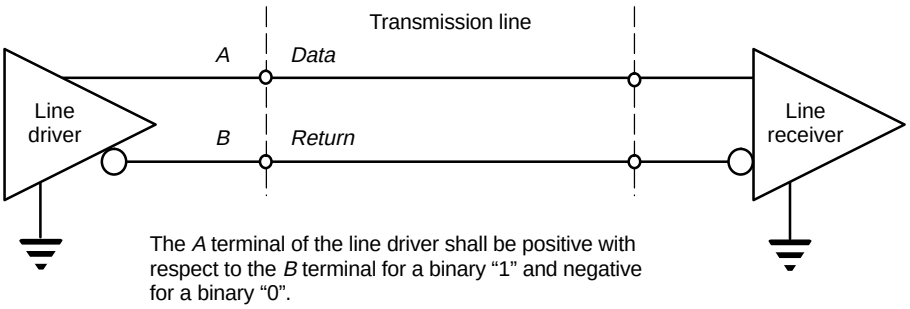
a) Clock–to–data timing relationship at the sending end.

Note:
The width of the window in the eye diagram (T_d), within which the data must be detected correctly, includes an allowance of:

± 3 ns	for clock jitter,
± 3 ns	for data timing variations, and
± 5 ns	for delay differences between signal pairs in the parallel interface cable.



b) Idealized eye diagram corresponding to the minimum input signal level.

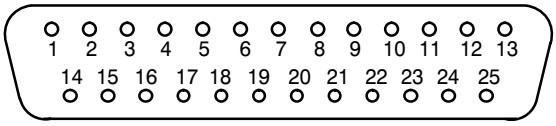


c) Convention defining the polarity of the binary signal.

Ref. 4 – Electrical characteristics of the parallel interface.

a) Connector contact assignments.

Old 8–bit system	Connector pin number	New 8–bit and 10–bit systems
Clock	1	Clock
System ground A	2	System ground A
Data 7 (MSB)	3	Data 9 (MSB)
Data 6	4	Data 8
Data 5	5	Data 7
Data 4	6	Data 6
Data 3	7	Data 5
Data 2	8	Data 4
Data 1	9	Data 3
Data 0	10	Data 2
Data A	11	Data 1
Data B	12	Data 0
Cable shield	13	Cable shield
Clock return	14	Clock return
System ground B	15	System ground B
Data 7 return	16	Data 9 return
Data 6 return	17	Data 8 return
Data 5 return	18	Data 7 return
Data 4 return	19	Data 6 return
Data 3 return	20	Data 5 return
Data 2 return	21	Data 4 return
Data 1 return	22	Data 3 return
Data 0 return	23	Data 2 return
Data A return	24	Data 1 return
Data B return	25	Data 0 return



b) Mating face of the 25–pin D–type connector receptacle (plug containing male pins).

Ref. 5 – Mechanical characteristics of the parallel interface.

a) Timing reference signal codes.

Data bit number	First word (FF)	Second word (00)	Third word (00)	Fourth word (XY)	Remarks
9	1	0	0	1	most–significant bit (MSB)
8	1	0	0	F	F = 0 in field 1 = 1 in field 2
7	1	0	0	V	V = 0 elsewhere = 1 during field blanking
6	1	0	0	H	H = 0 in *start of active video* (SAV) = 1 in *end of active video* (EAV)
5	1	0	0	P_3	Protection bits
4	1	0	0	P_2	
3	1	0	0	P_1	
2	1	0	0	P_0	
1	1	0	0	0	see *note 2*
0	1	0	0	0	

Notes:

1. The values shown are those recommended for 10–bit interfaces.

2. For compatibility with existing 8–bit interfaces, the values of bits D1 and D0 are not defined. These bits should be set to a fixed value and not left floating.

b) Structure of fourth TRS word (SAV, EAV).

Fourth word (XY)	First field				Second field			
	outside field blanking (V = 0)		during field blanking (V = 1)		outside field blanking (V = 0)		during field blanking (V = 1)	
	SAV	EAV	SAV	EAV	SAV	EAV	SAV	EAV
1 (MSB)	1	1	1	1	1	1	1	1
F	0	0	0	0	1	1	1	1
V	0	0	1	1	0	0	1	1
H	0	1	0	1	0	1	0	1
P_3	0	1	1	0	0	1	1	0
P_2	0	1	0	1	1	0	1	0
P_1	0	0	1	1	1	1	0	0
P_0	0	1	1	0	1	0	0	1
0	0	0	0	0	0	0	0	0
0 (LSB)	0	0	0	0	0	0	0	0
10–bit hex notation	80.0	9D.0	AB.0	B6.0	C7.0	DA.0	EC.0	F1.0

Ref. 6 – Timing reference signal.

Ref. 7 – Quantizing levels of the luminance channel (Y).

10–bit systems							Content	8–bit system			
Form 1			Form 2								
dec	hex	binary	binary	hex.hex	dec.dec	Voltage (mV)		Voltage (mV)	binary	hex	dec
		21 8421 8421	*8421 8421 84*		0.25/ step	0.799 mV/step		3.196 mV/step	*8421 8421*		
1023	3FF	11 1111 1111	1111 1111 11	FF.C	255.75	766.324	Forbidden in active picture	763.927	1111 1111	FF	255
.	.	.	.	.	.	.					
1020	3FC	11 1111 1100	1111 1111 00	FF.0	255.00	763.927					
1019	3FB	11 1111 1011	1111 1110 11	FE.C	254.75	763.128	Headroom	760.731	1111 1110	FE	254
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
941	3AD	11 1010 1101	1110 1011 01	EB.4	235.25	700.799		703.196	1110 1100	EC	236
940	3AC	11 1010 1100	1110 1011 00	EB.0	235.00	700.000	Nominal video level range	700.000	1110 1011	EB	235
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
64	40	00 0100 0000	0001 0000 00	10.0	16.00	0.000		0.000	0001 0000	10	16
63	3F	00 0011 1111	0000 1111 11	F.C	15.75	–0.799	Headroom	–3.196	0000 1111	F	15
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
4	4	00 0000 0100	0000 0001 00	1.0	1.00	–47.945		–47.945	0000 0001	1	1
3	3	00 0000 0011	0000 0000 11	0.C	0.75	–48.744	Forbidden in active picture				
.	.	.	.	.	.	.					
0	0	00 0000 0000	0000 0000 00	0.0	0.00	–51.142		–51.142	0000 0000	0	0

Ref. 8 – Quantizing levels of the chrominance channels (C_B, C_R).

10–bit systems							Content	8–bit system			
Form 1			Form 2								
dec	hex	binary	binary	hex.hex	dec.dec	Voltage (mV)		Voltage (mV)	binary	hex	dec
		21 8421 8421	*8421 8421 84*		0.25/ step	0.781 mV/step		3.125 mV/step	*8421 8421*		
1023	3FF	11 1111 1111	1111 1111 11	FF.C	255.75	399.219	Forbidden in active picture	396.875	1111 1111	FF	255
.	.	.	.	.	.	.					
1020	3FC	11 1111 1100	1111 1111 00	FF.0	255.00	396.875					
1019	3FB	11 1111 1011	1111 1110 11	FE.C	254.75	396.094	Headroom	393.750	1111 1110	FE	254
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
961	3C1	11 1100 0001	1111 0000 01	F0.4	240.25	350.781		353.125	1110 1100	EC	236
960	3C0	11 1100 0000	1111 0000 00	F0.0	240.00	350.000	Max. positive	350.000	1110 1011	EB	235
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.	Zero chrominance	.	.	.	.
512	200	10 0000 0000	1000 0000 00	80.0	128.00	0.000		0.000	1000 0000	80	128
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.	Max. negative	.	.	.	.
64	40	00 0100 0000	0001 0000 00	10.0	16.00	–350.000		–350.000	0001 0000	10	16
63	3F	00 0011 1111	0000 1111 11	F.C	15.75	–350.781	Headroom	–353.125	0000 1111	F	15
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.	.		.	.	.	.
4	4	00 0000 0100	0000 0001 00	1.0	1.00	–396.875		–396.875	0000 0001	1	1
3	3	00 0000 0011	0000 0000 11	0.C	0.75	–397.656	Forbidden in active picture				
.	.	.	.	.	.	.					
0	0	00 0000 0000	0000 0000 00	0.0	0.00	–400.000		–400.000	0000 0000	0	0

Ancillary data packet – Type 1

Ancillary data header (ADH)	Data ID *Type 1* (DID)	Data block number (DBN)	Data count (DC)	User data words (UDW) (see *note 1*)	Check–sum

Ancillary data packet – Type 2

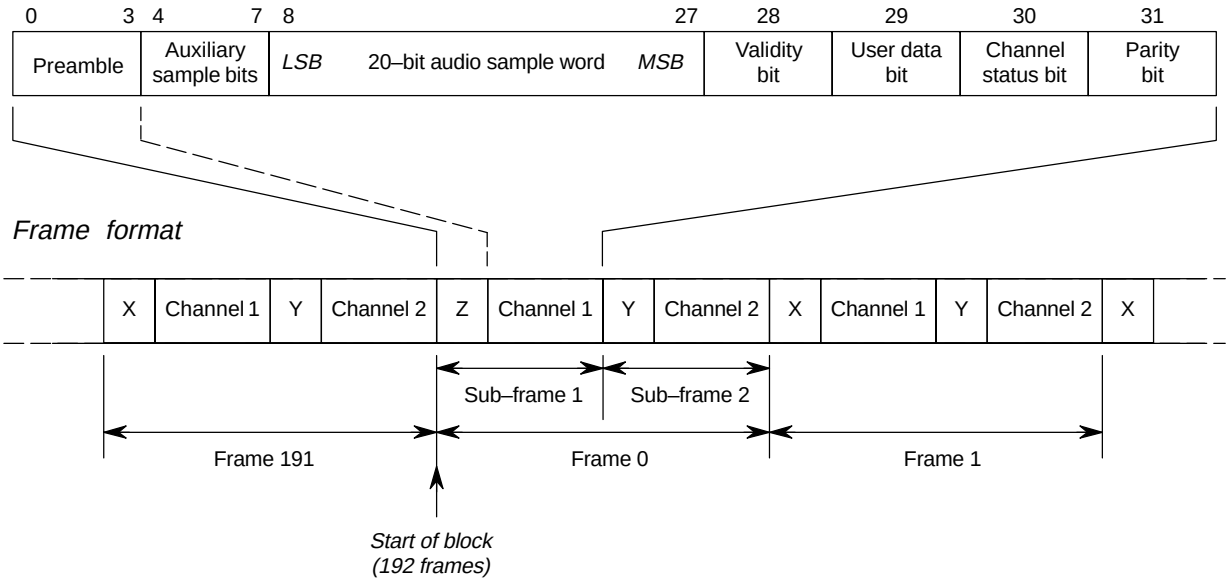
Ancillary data header (ADH)	Data ID *Type 2* (DID)	Secondary data ID (SDID)	Data count (DC)	User data words (UDW) (see *note 1*)	Check–sum

Notes:

1. The maximum length of an ancillary data packet is 255 bytes; the maximum number of user data words is 248.
2. Ancillary data is defined as 10–bit words, to maintain compatibility with the SDI signal format and interface.

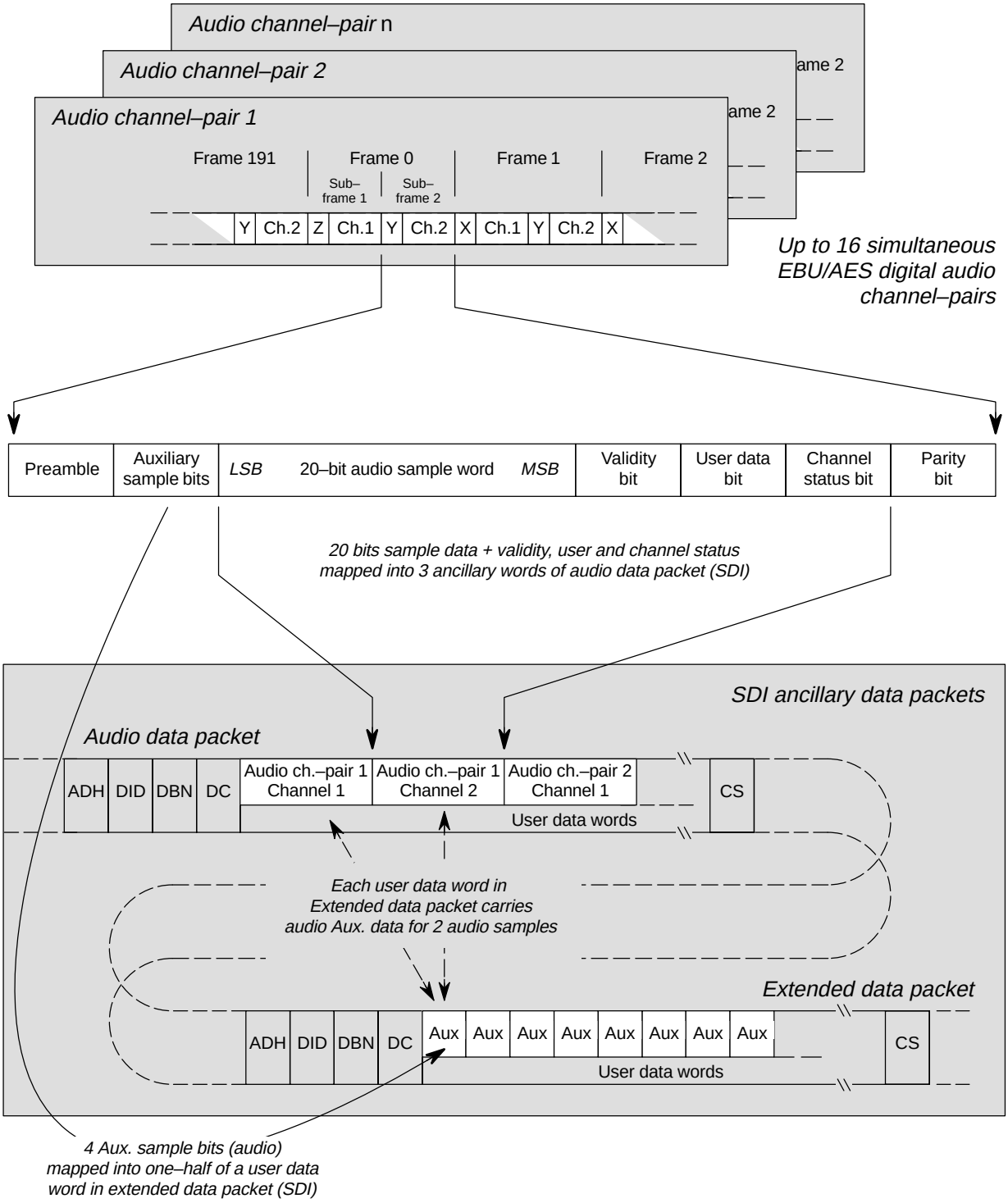
Ref. 9 – Ancillary data packet structure of the SDI.

Sub–frame format for audio sample words



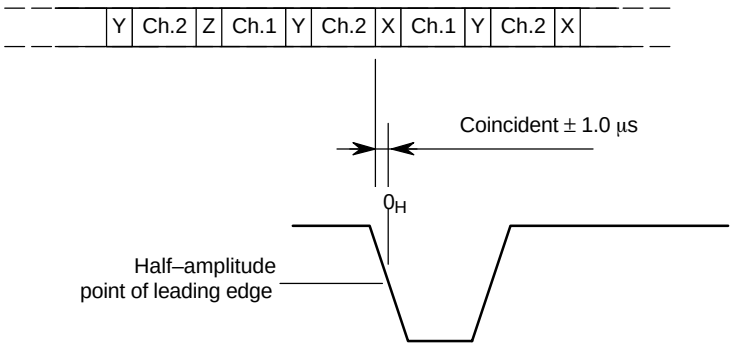
Note: The preamble contains synchronization data and can take one of three forms:
"X" Sub–frame 1
"Y" Sub–frame 2
"Z" Sub–frame 1 + block start

Ref. 10 – AES/EBU digital audio signal structure.



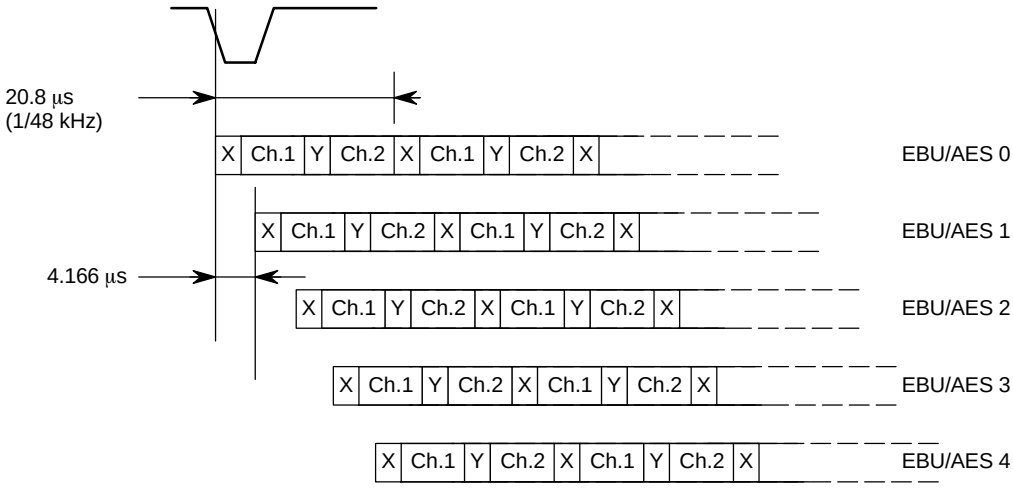
Note: The Audio data packet precedes the Extended data packet in the SDI data–stream.

Ref. 11 – Insertion of audio frames in ancillary data packets of the SDI

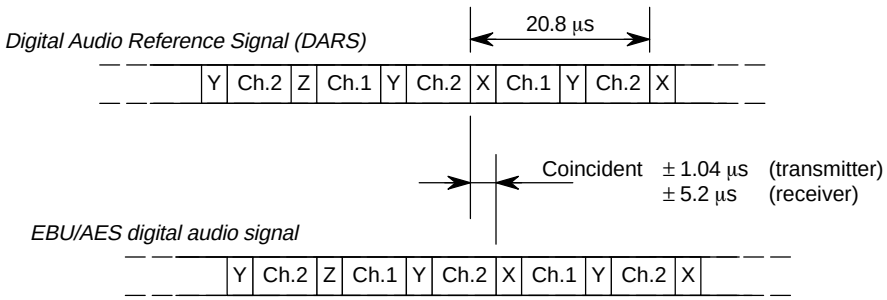


Note: 0_H is the video timing reference (see *Ref. 1*).

a) Timing relationship between digital audio and analogue video.



b) Digital audio sample phase, in the case of five EBU/AES audio channel–pairs.

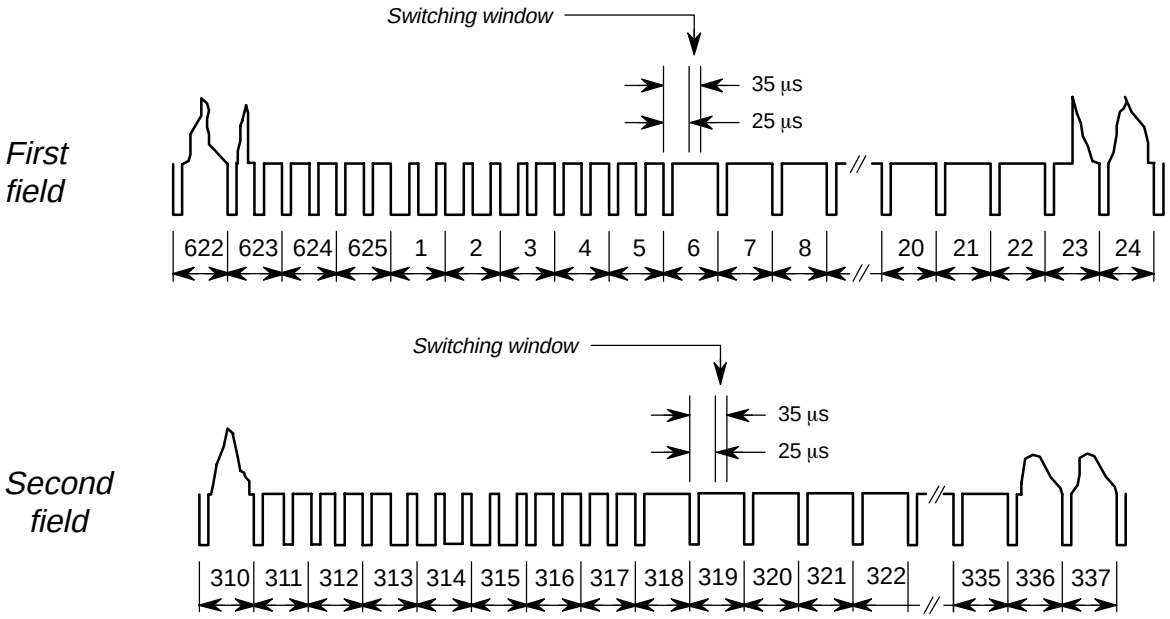


**c) Timing of EBU/AES digital audio channels
with respect to the digital audio reference signal (DARS).**

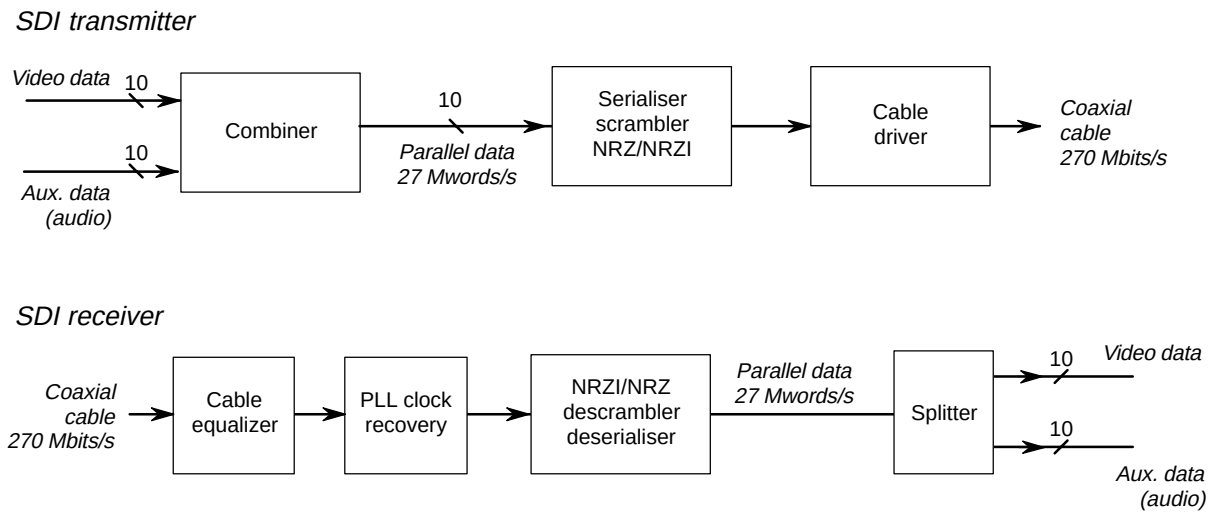
Ref. 12 – Timing of EBU/AES digital audio channels.

Ref. 13 – Digital time–code format

No. of word in 32–word message	Digital time–code information
0	00.X
1	FF.X
2	FF.X
3	49.X
4	15.X
5	TT3
6	LL1
7	LL2
8	Units of frames
9	First binary group
10	Tens of frames + Unassigned bit + Colour–lock flag bit
11	Second binary group
12	Units of seconds
13	Third binary group
14	Tens of seconds
15	Fourth binary group
16	Units of minutes
17	Fifth binary group
18	Tens of minutes + Binary group flag bit
19	Sixth binary group
20	Units of hours
21	Seventh binary group
22	Tens of hours + Unassigned bit + Field–mark bit
23	Eighth binary group
24	Units of months (optional)
25	Tens of months + 3 Unassigned bits (optional)
26	Units of days (optional)
27	Tens of days + 2 Unassigned bits (optional)
28	Units of years (optional)
29	Check on first data sub–group
30	Tens of years (optional)
31	Check on second data sub–group

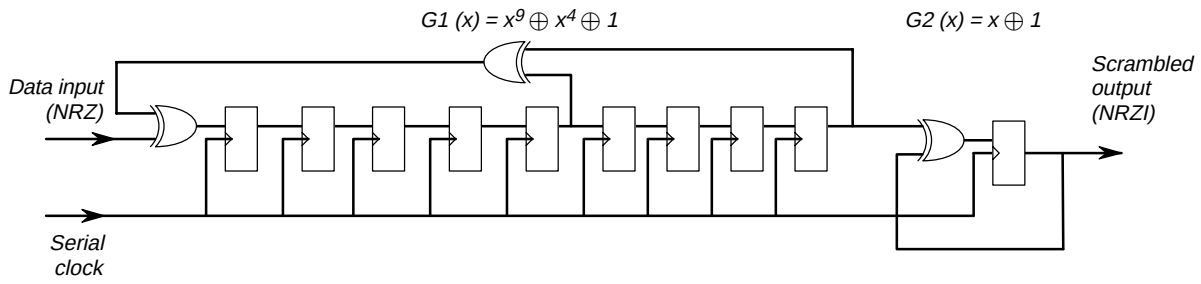


Ref. 14 – Switching window in the vertical blanking interval.

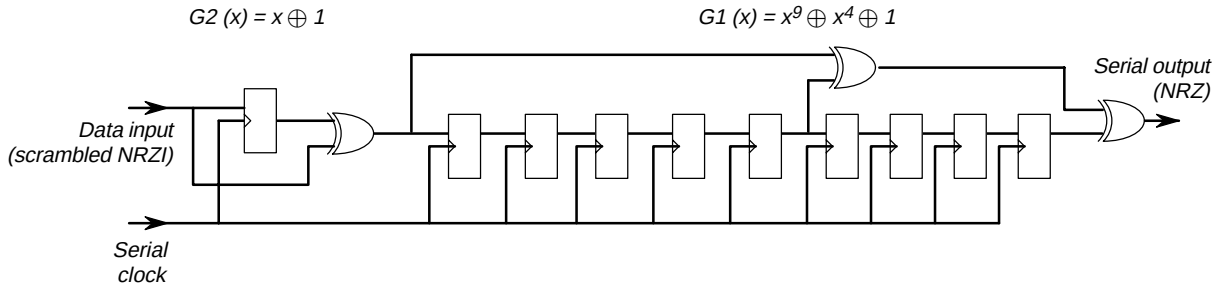


Ref. 15 – Typical block diagram of the SDI

Scrambler (NRZ to NRZI)



Decrambler (NRZI to NRZ)



Ref. 16 – Scrambling and coding in the SDI transmitter; decoding and descrambling in the SDI receiver

Model			
Receiver classification	B2	Transmitter classification	Standard

Key: RX: X: not recognised 0: recognised S: recognised and stored
TX: X: not transmitted 0: transmitted

Channel Status (C) data					
Byte	Bit	Function	RX	TX	Remarks
0	0	[0] Consumer use [1] Professional use	X O	X 0	
0	1	[0] Audio [1] Non audio	0 0	0 X	 Analogue O/P mutes (RX)
0	2–4 Emphasis	[000] Not indicated [100] No emphasis [110] 50/15 µs [111] CCITT J17	0 0 0 X	X 0 0 X	RX defaults to no emphasis RX defaults to no emphasis
0	5 Fs locked	[0] Locked [1] Unlocked	X X	0 X	
0	6–7 Sample freq.	[00] Not indicated [01] 48 kHz [10] 44.1 kHz [11] 32 kHz	0 0 0 X	X 0 0 X	Defaults to 48 kHz
1	0–3 Channel mode	[0000] Not indicated [0001] 2–channel [0010] Mono [0011] Prim/sec [0100] Stereo [0101–1111] Unidentified	0 0 0 0 0 X	X 0 X X X X	RX defaults to 2–channel mode Normal condition Ch A on both O/Ps RX defaults to 2–channel mode Same as 2–channel Don't care
1	4–7 User bit mode	[0000] Not indicated [0001] 192–bit block [0010] AES18 (HDLC) [0011] User defined [0100–1111] Unidentified	0 X X X X	0 X X X X	 Don't care
2	0–2 Aux. bit use	[000] Not indicated [001] Audio data [010] Coordination [011–111] Undefined	0 0 X X	0 X X X	 RX re–dithered to 16 bits
2	3–5 Sample length	[000] Not indicated [100] All other states	0 0 0	X 0 X	Default and re–ither to 16 bits 16 bits Re–dither to 16 bits
3	0–7	Multichannel modes	X	X	
4	0–1	AES 11 Source ID	X	X	
5	0–7	Unused	X	X	
6–9		ASCII Source ID	X	X	
10–13		ASCII Destination ID	X	X	
14–17		Local sample add code	X	X	
18–21		Time of day add code	X	X	
22	0–7	C reliability flags	X	X	
23	0–7	CRCC	0	0	
Validity (V) bit			S	0	
User (U) bit			X	X	
Audio sampling frequency (kHz)			44.1 / 48 (RX)	44.1 / 48 (TX)	
Audio sample word length (bits)			16–24, re–dithered to 16 (RX), 16 (TX)		

Ref. 17 – AES/EBU audio implementation chart

Ref. 18 – 8–bit luminance levels

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
1	01	−47.94	44	2C	89.49	87	57	226.9	130	82	364.3	173	AD	501.8
2	02	−44.74	45	2D	92.69	88	58	230.1	131	83	367.5	174	AE	505.0
3	03	−41.55	46	2E	95.89	89	59	233.3	132	84	370.7	175	AF	508.2
4	04	−38.35	47	2F	99.08	90	5A	236.5	133	85	373.9	176	B0	511.4
5	05	−35.15	48	30	102.2	91	5B	239.7	134	86	377.1	177	B1	514.6
6	06	−31.96	49	31	105.4	92	5C	242.9	135	87	380.3	178	B2	517.8
7	07	−28.76	50	32	108.6	93	5D	246.1	136	88	383.5	179	B3	521.0
8	08	−25.57	51	33	111.8	94	5E	249.3	137	89	386.7	180	B4	524.2
9	09	−22.37	52	34	115.0	95	5F	252.5	138	8A	389.9	181	B5	527.3
10	0A	−19.17	53	35	118.2	96	60	255.7	139	8B	393.1	182	B6	530.5
11	0B	−15.98	54	36	121.4	97	61	258.9	140	8C	396.3	183	B7	533.7
12	0C	−12.78	55	37	124.6	98	62	262.1	141	8D	399.5	184	B8	536.9
13	0D	−9.589	56	38	127.8	99	63	265.2	142	8E	402.7	185	B9	540.1
14	0E	−6.392	57	39	131.0	100	64	268.4	143	8F	405.9	186	BA	543.3
15	0F	−3.196	58	3A	134.2	101	65	271.6	144	90	409.1	187	BB	546.5
16	10	0	59	3B	137.4	102	66	274.8	145	91	412.3	188	BC	549.7
17	11	3.196	60	3C	140.6	103	67	278.0	146	92	415.5	189	BD	552.9
18	12	6.392	61	3D	143.8	104	68	281.2	147	93	418.7	190	BE	556.1
19	13	9.589	62	3E	147.0	105	69	284.4	148	94	421.9	191	BF	559.3
20	14	12.78	63	3F	150.2	106	6A	287.6	149	95	425.1	192	C0	562.5
21	15	15.98	64	40	153.4	107	6B	290.8	150	96	428.3	193	C1	565.7
22	16	19.17	65	41	156.6	108	6C	294.0	151	97	431.5	194	C2	568.9
23	17	22.37	66	42	159.8	109	6D	297.2	152	98	434.7	195	C3	572.1
24	18	25.57	67	43	163.0	110	6E	300.4	153	99	437.8	196	C4	575.3
25	19	28.76	68	44	166.2	111	6F	303.6	154	9A	441.0	197	C5	578.5
26	1A	31.96	69	45	169.4	112	70	306.8	155	9B	444.2	198	C6	581.7
27	1B	35.15	70	46	172.6	113	71	310.0	156	9C	447.4	199	C7	584.9
28	1C	38.35	71	47	175.7	114	72	313.2	157	9D	450.6	200	C8	588.1
29	1D	41.55	72	48	178.9	115	73	316.4	158	9E	453.8	201	C9	591.3
30	1E	44.74	73	49	182.1	116	74	319.6	159	9F	457.0	202	CA	594.5
31	1F	47.94	74	4A	185.3	117	75	322.8	160	A0	460.2	203	CB	597.7
32	20	51.14	75	4B	188.5	118	76	326.0	161	A1	463.4	204	CC	600.9
33	21	54.33	76	4C	191.7	119	77	329.2	162	A2	466.6	205	CD	604.1
34	22	57.53	77	4D	194.9	120	78	332.4	163	A3	469.8	206	CE	607.3
35	23	60.73	78	4E	198.1	121	79	335.6	164	A4	473.0	207	CF	610.5
36	24	63.92	79	4F	201.3	122	7A	338.8	165	A5	476.2	208	D0	613.6
37	25	67.12	80	50	204.5	123	7B	342.0	166	A6	479.4	209	D1	616.8
38	26	70.31	81	51	207.7	124	7C	345.2	167	A7	482.6	210	D2	620.0
39	27	73.51	82	52	210.9	125	7D	348.4	168	A8	485.8	211	D3	623.2
40	28	76.71	83	53	214.1	126	7E	351.5	169	A9	489.0	212	D4	626.4
41	29	79.90	84	54	217.3	127	7F	354.7	170	AA	492.2	213	D5	629.6
42	2A	83.10	85	55	220.5	128	80	357.9	171	AB	495.4	214	D6	632.8
43	2B	86.30	86	56	223.7	129	81	361.1	172	AC	498.6	215	D7	636.0

Ref. 18 – 8–bit luminance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
216	D8	639.2	224	E0	664.8	232	E8	690.4	240	F0	715.9	248	F8	741.5
217	D9	642.4	225	E1	668.0	233	E9	693.6	241	F1	719.1	249	F9	744.7
218	DA	645.6	226	E2	671.2	234	EA	696.8	242	F2	722.3	250	FA	747.9
219	DB	648.8	227	E3	674.4	235	EB	700.0	243	F3	725.5	251	FB	751.1
220	DC	652.0	228	E4	677.6	236	EC	703.1	244	F4	728.7	252	FC	754.3
221	DD	655.2	229	E5	680.8	237	ED	706.3	245	F5	731.9	253	FD	757.5
222	DE	658.4	230	E6	684.0	238	EE	709.5	246	F6	735.1	254	FE	760.7
223	DF	661.6	231	E7	687.2	239	EF	712.7	247	F7	738.3			

Ref. 19 – 8–bit chrominance levels

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
1	01	–396.8	44	2C	–262.5	87	57	–128.1	130	82	6.250	173	AD	140.6
2	02	–393.7	45	2D	–259.3	88	58	–125.0	131	83	9.375	174	AE	143.7
3	03	–390.6	46	2E	–256.2	89	59	–121.8	132	84	12.50	175	AF	146.8
4	04	–387.5	47	2F	–253.1	90	5A	–118.7	133	85	15.62	176	B0	150.0
5	05	–384.3	48	30	–250.0	91	5B	–115.6	134	86	18.75	177	B1	153.1
6	06	–381.2	49	31	–246.8	92	5C	–112.5	135	87	21.87	178	B2	156.2
7	07	–378.1	50	32	–243.7	93	5D	–109.3	136	88	25.00	179	B3	159.3
8	08	–375.0	51	33	–240.6	94	5E	–106.2	137	89	28.12	180	B4	162.5
9	09	–371.8	52	34	–237.5	95	5F	–103.1	138	8A	31.25	181	B5	165.6
10	0A	–368.7	53	35	–234.3	96	60	–100.0	139	8B	34.37	182	B6	168.7
11	0B	–365.6	54	36	–231.2	97	61	–96.87	140	8C	37.50	183	B7	171.8
12	0C	–362.5	55	37	–228.1	98	62	–93.75	141	8D	40.62	184	B8	175.0
13	0D	–359.3	56	38	–225.0	99	63	–90.62	142	8E	43.75	185	B9	178.1
14	0E	–356.2	57	39	–221.8	100	64	–87.50	143	8F	46.87	186	BA	181.2
15	0F	–353.1	58	3A	–218.7	101	65	–84.37	144	90	50.00	187	BB	184.3
16	10	–350.0	59	3B	–215.6	102	66	–81.25	145	91	53.12	188	BC	187.5
17	11	–346.8	60	3C	–212.5	103	67	–78.12	146	92	56.25	189	BD	190.6
18	12	–343.7	61	3D	–209.3	104	68	–75.00	147	93	59.37	190	BE	193.7
19	13	–340.6	62	3E	–206.2	105	69	–71.87	148	94	62.50	191	BF	196.8
20	14	–337.5	63	3F	–203.1	106	6A	–68.75	149	95	65.62	192	C0	200.0
21	15	–334.3	64	40	–200.0	107	6B	–65.62	150	96	68.75	193	C1	203.1
22	16	–331.2	65	41	–196.8	108	6C	–62.50	151	97	71.87	194	C2	206.2
23	17	–328.1	66	42	–193.7	109	6D	–59.37	152	98	75.00	195	C3	209.3
24	18	–325.0	67	43	–190.6	110	6E	–56.25	153	99	78.12	196	C4	212.5
25	19	–321.8	68	44	–187.5	111	6F	–53.12	154	9A	81.25	197	C5	215.6
26	1A	–318.7	69	45	–184.3	112	70	–50.00	155	9B	84.37	198	C6	218.7
27	1B	–315.6	70	46	–181.2	113	71	–46.87	156	9C	87.50	199	C7	221.8
28	1C	–312.5	71	47	–178.1	114	72	–43.75	157	9D	90.62	200	C8	225.0
29	1D	–309.3	72	48	–175.0	115	73	–40.62	158	9E	93.75	201	C9	228.1
30	1E	–306.2	73	49	–171.8	116	74	–37.50	159	9F	96.87	202	CA	231.2
31	1F	–303.1	74	4A	–168.7	117	75	–34.37	160	A0	100.0	203	CB	234.3
32	20	–300.0	75	4B	–165.6	118	76	–31.25	161	A1	103.1	204	CC	237.5
33	21	–296.8	76	4C	–162.5	119	77	–28.12	162	A2	106.2	205	CD	240.6
34	22	–293.7	77	4D	–159.3	120	78	–25.00	163	A3	109.3	206	CE	243.7
35	23	–290.6	78	4E	–156.2	121	79	–21.87	164	A4	112.5	207	CF	246.8
36	24	–287.5	79	4F	–153.1	122	7A	–18.75	165	A5	115.6	208	D0	250.0
37	25	–284.3	80	50	–150.0	123	7B	–15.62	166	A6	118.7	209	D1	253.1
38	26	–281.2	81	51	–146.8	124	7C	–12.50	167	A7	121.8	210	D2	256.2
39	27	–278.1	82	52	–143.7	125	7D	–9.375	168	A8	125.0	211	D3	259.3
40	28	–275.0	83	53	–140.6	126	7E	–6.250	169	A9	128.1	212	D4	262.5
41	29	–271.8	84	54	–137.5	127	7F	–3.125	170	AA	131.2	213	D5	265.6
42	2A	–268.7	85	55	–134.3	128	80	0.000	171	AB	134.3	214	D6	268.7
43	2B	–265.6	86	56	–131.2	129	81	3.125	172	AC	137.5	215	D7	271.8

Ref. 19 – 8–bit chrominance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
216	D8	275.0	224	E0	300.0	232	E8	325.0	240	F0	350.0	248	F8	375.0
217	D9	278.1	225	E1	303.1	233	E9	328.1	241	F1	353.1	249	F9	378.1
218	DA	281.2	226	E2	306.2	234	EA	331.2	242	F2	356.2	250	FA	381.2
219	DB	284.3	227	E3	309.3	235	EB	334.3	243	F3	359.3	251	FB	384.3
220	DC	287.5	228	E4	312.5	236	EC	337.5	244	F4	362.5	252	FC	387.5
221	DD	290.6	229	E5	315.6	237	ED	340.6	245	F5	365.6	253	FD	390.6
222	DE	293.7	230	E6	318.7	238	EE	343.7	246	F6	368.7	254	FE	393.7
223	DF	296.8	231	E7	321.8	239	EF	346.8	247	F7	371.8			

Ref. 20 – 10–bit luminance levels

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
			12.00	0C.0	−12.785	24.00	18.0	25.570	36.00	24.0	63.926	48.00	30.0	102.28
			12.25	0C.4	−11.986	24.25	18.4	26.369	36.25	24.4	64.726	48.25	30.4	103.08
			12.50	0C.8	−11.187	24.50	18.8	27.168	36.50	24.8	65.525	48.50	30.8	103.88
			12.75	0C.C	−10.388	24.75	18.C	27.968	36.75	24.C	66.324	48.75	30.C	104.68
1.00	01.0	−47.945	13.00	0D.0	−9.5890	25.00	19.0	28.767	37.00	25.0	67.123	49.00	31.0	105.47
1.25	01.4	−47.146	13.25	0D.4	−8.7899	25.25	19.4	29.566	37.25	25.4	67.922	49.25	31.4	106.27
1.50	01.8	−46.347	13.50	0D.8	−7.9908	25.50	19.8	30.365	37.50	25.8	68.721	49.50	31.8	107.07
1.75	01.C	−45.547	13.75	0D.C	−7.1917	25.75	19.C	31.164	37.75	25.C	69.520	49.75	31.C	107.87
2.00	02.0	−44.748	14.00	0E.0	−6.3926	26.00	1A.0	31.963	38.00	26.0	70.319	50.00	32.0	108.67
2.25	02.4	−43.949	14.25	0E.4	−5.5936	26.25	1A.4	32.762	38.25	26.4	71.118	50.25	32.4	109.47
2.50	02.8	−43.150	14.50	0E.8	−4.7945	26.50	1A.8	33.561	38.50	26.8	71.917	50.50	32.8	110.27
2.75	02.C	−42.351	14.75	0E.C	−3.9954	26.75	1A.C	34.360	38.75	26.C	72.716	50.75	32.C	111.07
3.00	03.0	−41.552	15.00	0F.0	−3.1963	27.00	1B.0	35.159	39.00	27.0	73.516	51.00	33.0	111.87
3.25	03.4	−40.753	15.25	0F.4	−2.3972	27.25	1B.4	35.958	39.25	27.4	74.315	51.25	33.4	112.67
3.50	03.8	−39.954	15.50	0F.8	−1.5981	27.50	1B.8	36.758	39.50	27.8	75.114	51.50	33.8	113.47
3.75	03.C	−39.155	15.75	0F.C	−.79908	27.75	1B.C	37.557	39.75	27.C	75.913	51.75	33.C	114.26
4.00	04.0	−38.356	16.00	10.0	0	28.00	1C.0	38.356	40.00	28.0	76.712	52.00	34.0	115.06
4.25	04.4	−37.557	16.25	10.4	.79908	28.25	1C.4	39.155	40.25	28.4	77.511	52.25	34.4	115.86
4.50	04.8	−36.758	16.50	10.8	1.5981	28.50	1C.8	39.954	40.50	28.8	78.310	52.50	34.8	116.66
4.75	04.C	−35.958	16.75	10.C	2.3972	28.75	1C.C	40.753	40.75	28.C	79.109	52.75	34.C	117.46
5.00	05.0	−35.159	17.00	11.0	3.1963	29.00	1D.0	41.552	41.00	29.0	79.908	53.00	35.0	118.26
5.25	05.4	−34.360	17.25	11.4	3.9954	29.25	1D.4	42.351	41.25	29.4	80.707	53.25	35.4	119.06
5.50	05.8	−33.561	17.50	11.8	4.7945	29.50	1D.8	43.150	41.50	29.8	81.506	53.50	35.8	119.86
5.75	05.C	−32.762	17.75	11.C	5.5936	29.75	1D.C	43.949	41.75	29.C	82.305	53.75	35.C	120.66
6.00	06.0	−31.963	18.00	12.0	6.3926	30.00	1E.0	44.748	42.00	2A.0	83.105	54.00	36.0	121.46
6.25	06.4	−31.164	18.25	12.4	7.1917	30.25	1E.4	45.547	42.25	2A.4	83.904	54.25	36.4	122.26
6.50	06.8	−30.365	18.50	12.8	7.9908	30.50	1E.8	46.347	42.50	2A.8	84.703	54.50	36.8	123.05
6.75	06.C	−29.566	18.75	12.C	8.7899	30.75	1E.C	47.146	42.75	2A.C	85.502	54.75	36.C	123.85
7.00	07.0	−28.767	19.00	13.0	9.5890	31.00	1F.0	47.945	43.00	2B.0	86.301	55.00	37.0	124.65
7.25	07.4	−27.968	19.25	13.4	10.388	31.25	1F.4	48.744	43.25	2B.4	87.100	55.25	37.4	125.45
7.50	07.8	−27.168	19.50	13.8	11.187	31.50	1F.8	49.543	43.50	2B.8	87.899	55.50	37.8	126.25
7.75	07.C	−26.369	19.75	13.C	11.986	31.75	1F.C	50.342	43.75	2B.C	88.698	55.75	37.C	127.05
8.00	08.0	−25.570	20.00	14.0	12.785	32.00	20.0	51.141	44.00	2C.0	89.497	56.00	38.0	127.85
8.25	08.4	−24.771	20.25	14.4	13.584	32.25	20.4	51.940	44.25	2C.4	90.296	56.25	38.4	128.65
8.50	08.8	−23.972	20.50	14.8	14.383	32.50	20.8	52.739	44.50	2C.8	91.095	56.50	38.8	129.45
8.75	08.C	−23.173	20.75	14.C	15.182	32.75	20.C	53.538	44.75	2C.C	91.895	56.75	38.C	130.25
9.00	09.0	−22.374	21.00	15.0	15.981	33.00	21.0	54.337	45.00	2D.0	92.694	57.00	39.0	131.05
9.25	09.4	−21.575	21.25	15.4	16.780	33.25	21.4	55.137	45.25	2D.4	93.493	57.25	39.4	131.84
9.50	09.8	−20.776	21.50	15.8	17.579	33.50	21.8	55.936	45.50	2D.8	94.292	57.50	39.8	132.64
9.75	09.C	−19.977	21.75	15.C	18.379	33.75	21.C	56.735	45.75	2D.C	95.091	57.75	39.C	133.44
10.00	0A.0	−19.178	22.00	16.0	19.178	34.00	22.0	57.534	46.00	2E.0	95.890	58.00	3A.0	134.24
10.25	0A.4	−18.379	22.25	16.4	19.977	34.25	22.4	58.333	46.25	2E.4	96.689	58.25	3A.4	135.04
10.50	0A.8	−17.579	22.50	16.8	20.776	34.50	22.8	59.132	46.50	2E.8	97.488	58.50	3A.8	135.84
10.75	0A.C	−16.780	22.75	16.C	21.575	34.75	22.C	59.931	46.75	2E.C	98.287	58.75	3A.C	136.64
11.00	0B.0	−15.981	23.00	17.0	22.374	35.00	23.0	60.730	47.00	2F.0	99.086	59.00	3B.0	137.44
11.25	0B.4	−15.182	23.25	17.4	23.173	35.25	23.4	61.529	47.25	2F.4	99.885	59.25	3B.4	138.24
11.50	0B.8	−14.383	23.50	17.8	23.972	35.50	23.8	62.328	47.50	2F.8	100.68	59.50	3B.8	139.04
11.75	0B.C	−13.584	23.75	17.C	24.771	35.75	23.C	63.127	47.75	2F.C	101.48	59.75	3B.C	139.84

Ref. 20 – 10–bit luminance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
60.00	3C.0	140.63	72.00	48.0	178.99	84.00	54.0	217.35	96.00	60.0	255.70	108.00	6C.0	294.06
60.25	3C.4	141.43	72.25	48.4	179.79	84.25	54.4	218.15	96.25	60.4	256.50	108.25	6C.4	294.86
60.50	3C.8	142.23	72.50	48.8	180.59	84.50	54.8	218.94	96.50	60.8	257.30	108.50	6C.8	295.66
60.75	3C.C	143.03	72.75	48.C	181.39	84.75	54.C	219.74	96.75	60.C	258.10	108.75	6C.C	296.46
61.00	3D.0	143.83	73.00	49.0	182.19	85.00	55.0	220.54	97.00	61.0	258.90	109.00	6D.0	297.26
61.25	3D.4	144.63	73.25	49.4	182.99	85.25	55.4	221.34	97.25	61.4	259.70	109.25	6D.4	298.05
61.50	3D.8	145.43	73.50	49.8	183.79	85.50	55.8	222.14	97.50	61.8	260.50	109.50	6D.8	298.85
61.75	3D.C	146.23	73.75	49.C	184.58	85.75	55.C	222.94	97.75	61.C	261.30	109.75	6D.C	299.65
62.00	3E.0	147.03	74.00	4A.0	185.38	86.00	56.0	223.74	98.00	62.0	262.10	110.00	6E.0	300.45
62.25	3E.4	147.83	74.25	4A.4	186.18	86.25	56.4	224.54	98.25	62.4	262.89	110.25	6E.4	301.25
62.50	3E.8	148.63	74.50	4A.8	186.98	86.50	56.8	225.34	98.50	62.8	263.69	110.50	6E.8	302.05
62.75	3E.C	149.42	74.75	4A.C	187.78	86.75	56.C	226.14	98.75	62.C	264.49	110.75	6E.C	302.85
63.00	3F.0	150.22	75.00	4B.0	188.58	87.00	57.0	226.94	99.00	63.0	265.29	111.00	6F.0	303.65
63.25	3F.4	151.02	75.25	4B.4	189.38	87.25	57.4	227.73	99.25	63.4	266.09	111.25	6F.4	304.45
63.50	3F.8	151.82	75.50	4B.8	190.18	87.50	57.8	228.53	99.50	63.8	266.89	111.50	6F.8	305.25
63.75	3F.C	152.62	75.75	4B.C	190.98	87.75	57.C	229.33	99.75	63.C	267.69	111.75	6F.C	306.05
64.00	40.0	153.42	76.00	4C.0	191.78	88.00	58.0	230.13	100.00	64.0	268.49	112.00	70.0	306.84
64.25	40.4	154.22	76.25	4C.4	192.57	88.25	58.4	230.93	100.25	64.4	269.29	112.25	70.4	307.64
64.50	40.8	155.02	76.50	4C.8	193.37	88.50	58.8	231.73	100.50	64.8	270.09	112.50	70.8	308.44
64.75	40.C	155.82	76.75	4C.C	194.17	88.75	58.C	232.53	100.75	64.C	270.89	112.75	70.C	309.24
65.00	41.0	156.62	77.00	4D.0	194.97	89.00	59.0	233.33	101.00	65.0	271.68	113.00	71.0	310.04
65.25	41.4	157.42	77.25	4D.4	195.77	89.25	59.4	234.13	101.25	65.4	272.48	113.25	71.4	310.84
65.50	41.8	158.21	77.50	4D.8	196.57	89.50	59.8	234.93	101.50	65.8	273.28	113.50	71.8	311.64
65.75	41.C	159.01	77.75	4D.C	197.37	89.75	59.C	235.73	101.75	65.C	274.08	113.75	71.C	312.44
66.00	42.0	159.81	78.00	4E.0	198.17	90.00	5A.0	236.52	102.00	66.0	274.88	114.00	72.0	313.24
66.25	42.4	160.61	78.25	4E.4	198.97	90.25	5A.4	237.32	102.25	66.4	275.68	114.25	72.4	314.04
66.50	42.8	161.41	78.50	4E.8	199.77	90.50	5A.8	238.12	102.50	66.8	276.48	114.50	72.8	314.84
66.75	42.C	162.21	78.75	4E.C	200.57	90.75	5A.C	238.92	102.75	66.C	277.28	114.75	72.C	315.63
67.00	43.0	163.01	79.00	4F.0	201.36	91.00	5B.0	239.72	103.00	67.0	278.08	115.00	73.0	316.43
67.25	43.4	163.81	79.25	4F.4	202.16	91.25	5B.4	240.52	103.25	67.4	278.88	115.25	73.4	317.23
67.50	43.8	164.61	79.50	4F.8	202.96	91.50	5B.8	241.32	103.50	67.8	279.68	115.50	73.8	318.03
67.75	43.C	165.41	79.75	4F.C	203.76	91.75	5B.C	242.12	103.75	67.C	280.47	115.75	73.C	318.83
68.00	44.0	166.21	80.00	50.0	204.56	92.00	5C.0	242.92	104.00	68.0	281.27	116.00	74.0	319.63
68.25	44.4	167.00	80.25	50.4	205.36	92.25	5C.4	243.72	104.25	68.4	282.07	116.25	74.4	320.43
68.50	44.8	167.80	80.50	50.8	206.16	92.50	5C.8	244.52	104.50	68.8	282.87	116.50	74.8	321.23
68.75	44.C	168.60	80.75	50.C	206.96	92.75	5C.C	245.31	104.75	68.C	283.67	116.75	74.C	322.03
69.00	45.0	169.40	81.00	51.0	207.76	93.00	5D.0	246.11	105.00	69.0	284.47	117.00	75.0	322.83
69.25	45.4	170.20	81.25	51.4	208.56	93.25	5D.4	246.91	105.25	69.4	285.27	117.25	75.4	323.63
69.50	45.8	171.00	81.50	51.8	209.36	93.50	5D.8	247.71	105.50	69.8	286.07	117.50	75.8	324.42
69.75	45.C	171.80	81.75	51.C	210.15	93.75	5D.C	248.51	105.75	69.C	286.87	117.75	75.C	325.22
70.00	46.0	172.60	82.00	52.0	210.95	94.00	5E.0	249.31	106.00	6A.0	287.67	118.00	76.0	326.02
70.25	46.4	173.40	82.25	52.4	211.75	94.25	5E.4	250.11	106.25	6A.4	288.47	118.25	76.4	326.82
70.50	46.8	174.20	82.50	52.8	212.55	94.50	5E.8	250.91	106.50	6A.8	289.26	118.50	76.8	327.62
70.75	46.C	175.00	82.75	52.C	213.35	94.75	5E.C	251.71	106.75	6A.C	290.06	118.75	76.C	328.42
71.00	47.0	175.79	83.00	53.0	214.15	95.00	5F.0	252.51	107.00	6B.0	290.86	119.00	77.0	329.22
71.25	47.4	176.59	83.25	53.4	214.95	95.25	5F.4	253.31	107.25	6B.4	291.66	119.25	77.4	330.02
71.50	47.8	177.39	83.50	53.8	215.75	95.50	5F.8	254.10	107.50	6B.8	292.46	119.50	77.8	330.82
71.75	47.C	178.19	83.75	53.C	216.55	95.75	5F.C	254.90	107.75	6B.C	293.26	119.75	77.C	331.62

Ref. 20 – 10–bit luminance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
120.00	78.0	332.42	132.00	84.0	370.77	144.00	90.0	409.13	156.00	9C.0	447.48	168.00	A8.0	485.84
120.25	78.4	333.21	132.25	84.4	371.57	144.25	90.4	409.93	156.25	9C.4	448.28	168.25	A8.4	486.64
120.50	78.8	334.01	132.50	84.8	372.37	144.50	90.8	410.73	156.50	9C.8	449.08	168.50	A8.8	487.44
120.75	78.C	334.81	132.75	84.C	373.17	144.75	90.C	411.52	156.75	9C.C	449.88	168.75	A8.C	488.24
121.00	79.0	335.61	133.00	85.0	373.97	145.00	91.0	412.32	157.00	9D.0	450.68	169.00	A9.0	489.04
121.25	79.4	336.41	133.25	85.4	374.77	145.25	91.4	413.12	157.25	9D.4	451.48	169.25	A9.4	489.84
121.50	79.8	337.21	133.50	85.8	375.57	145.50	91.8	413.92	157.50	9D.8	452.28	169.50	A9.8	490.63
121.75	79.C	338.01	133.75	85.C	376.36	145.75	91.C	414.72	157.75	9D.C	453.08	169.75	A9.C	491.43
122.00	7A.0	338.81	134.00	86.0	377.16	146.00	92.0	415.52	158.00	9E.0	453.88	170.00	AA.0	492.23
122.25	7A.4	339.61	134.25	86.4	377.96	146.25	92.4	416.32	158.25	9E.4	454.68	170.25	AA.4	493.03
122.50	7A.8	340.41	134.50	86.8	378.76	146.50	92.8	417.12	158.50	9E.8	455.47	170.50	AA.8	493.83
122.75	7A.C	341.21	134.75	86.C	379.56	146.75	92.C	417.92	158.75	9E.C	456.27	170.75	AA.C	494.63
123.00	7B.0	342.00	135.00	87.0	380.36	147.00	93.0	418.72	159.00	9F.0	457.07	171.00	AB.0	495.43
123.25	7B.4	342.80	135.25	87.4	381.16	147.25	93.4	419.52	159.25	9F.4	457.87	171.25	AB.4	496.23
123.50	7B.8	343.60	135.50	87.8	381.96	147.50	93.8	420.31	159.50	9F.8	458.67	171.50	AB.8	497.03
123.75	7B.C	344.40	135.75	87.C	382.76	147.75	93.C	421.11	159.75	9F.C	459.47	171.75	AB.C	497.83
124.00	7C.0	345.20	136.00	88.0	383.56	148.00	94.0	421.91	160.00	A0.0	460.27	172.00	AC.0	498.63
124.25	7C.4	346.00	136.25	88.4	384.36	148.25	94.4	422.71	160.25	A0.4	461.07	172.25	AC.4	499.42
124.50	7C.8	346.80	136.50	88.8	385.15	148.50	94.8	423.51	160.50	A0.8	461.87	172.50	AC.8	500.22
124.75	7C.C	347.60	136.75	88.C	385.95	148.75	94.C	424.31	160.75	A0.C	462.67	172.75	AC.C	501.02
125.00	7D.0	348.40	137.00	89.0	386.75	149.00	95.0	425.11	161.00	A1.0	463.47	173.00	AD.0	501.82
125.25	7D.4	349.20	137.25	89.4	387.55	149.25	95.4	425.91	161.25	A1.4	464.26	173.25	AD.4	502.62
125.50	7D.8	350.00	137.50	89.8	388.35	149.50	95.8	426.71	161.50	A1.8	465.06	173.50	AD.8	503.42
125.75	7D.C	350.79	137.75	89.C	389.15	149.75	95.C	427.51	161.75	A1.C	465.86	173.75	AD.C	504.22
126.00	7E.0	351.59	138.00	8A.0	389.95	150.00	96.0	428.31	162.00	A2.0	466.66	174.00	AE.0	505.02
126.25	7E.4	352.39	138.25	8A.4	390.75	150.25	96.4	429.10	162.25	A2.4	467.46	174.25	AE.4	505.82
126.50	7E.8	353.19	138.50	8A.8	391.55	150.50	96.8	429.90	162.50	A2.8	468.26	174.50	AE.8	506.62
126.75	7E.C	353.99	138.75	8A.C	392.35	150.75	96.C	430.70	162.75	A2.C	469.06	174.75	AE.C	507.42
127.00	7F.0	354.79	139.00	8B.0	393.15	151.00	97.0	431.50	163.00	A3.0	469.86	175.00	AF.0	508.21
127.25	7F.4	355.59	139.25	8B.4	393.94	151.25	97.4	432.30	163.25	A3.4	470.66	175.25	AF.4	509.01
127.50	7F.8	356.39	139.50	8B.8	394.74	151.50	97.8	433.10	163.50	A3.8	471.46	175.50	AF.8	509.81
127.75	7F.C	357.19	139.75	8B.C	395.54	151.75	97.C	433.90	163.75	A3.C	472.26	175.75	AF.C	510.61
128.00	80.0	357.99	140.00	8C.0	396.34	152.00	98.0	434.70	164.00	A4.0	473.05	176.00	B0.0	511.41
128.25	80.4	358.79	140.25	8C.4	397.14	152.25	98.4	435.50	164.25	A4.4	473.85	176.25	B0.4	512.21
128.50	80.8	359.58	140.50	8C.8	397.94	152.50	98.8	436.30	164.50	A4.8	474.65	176.50	B0.8	513.01
128.75	80.C	360.38	140.75	8C.C	398.74	152.75	98.C	437.10	164.75	A4.C	475.45	176.75	B0.C	513.81
129.00	81.0	361.18	141.00	8D.0	399.54	153.00	99.0	437.89	165.00	A5.0	476.25	177.00	B1.0	514.61
129.25	81.4	361.98	141.25	8D.4	400.34	153.25	99.4	438.69	165.25	A5.4	477.05	177.25	B1.4	515.41
129.50	81.8	362.78	141.50	8D.8	401.14	153.50	99.8	439.49	165.50	A5.8	477.85	177.50	B1.8	516.21
129.75	81.C	363.58	141.75	8D.C	401.94	153.75	99.C	440.29	165.75	A5.C	478.65	177.75	B1.C	517.00
130.00	82.0	364.38	142.00	8E.0	402.73	154.00	9A.0	441.09	166.00	A6.0	479.45	178.00	B2.0	517.80
130.25	82.4	365.18	142.25	8E.4	403.53	154.25	9A.4	441.89	166.25	A6.4	480.25	178.25	B2.4	518.60
130.50	82.8	365.98	142.50	8E.8	404.33	154.50	9A.8	442.69	166.50	A6.8	481.05	178.50	B2.8	519.40
130.75	82.C	366.78	142.75	8E.C	405.13	154.75	9A.C	443.49	166.75	A6.C	481.84	178.75	B2.C	520.20
131.00	83.0	367.58	143.00	8F.0	405.93	155.00	9B.0	444.29	167.00	A7.0	482.64	179.00	B3.0	521.00
131.25	83.4	368.37	143.25	8F.4	406.73	155.25	9B.4	445.09	167.25	A7.4	483.44	179.25	B3.4	521.80
131.50	83.8	369.17	143.50	8F.8	407.53	155.50	9B.8	445.89	167.50	A7.8	484.24	179.50	B3.8	522.60
131.75	83.C	369.97	143.75	8F.C	408.33	155.75	9B.C	446.68	167.75	A7.C	485.04	179.75	B3.C	523.40

Ref. 20 – 10–bit luminance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
180.00	B4.0	524.20	192.00	C0.0	562.55	204.00	CC.0	600.91	216.00	D8.0	639.26	228.00	E4.0	677.62
180.25	B4.4	525.00	192.25	C0.4	563.35	204.25	CC.4	601.71	216.25	D8.4	640.06	228.25	E4.4	678.42
180.50	B4.8	525.79	192.50	C0.8	564.15	204.50	CC.8	602.51	216.50	D8.8	640.86	228.50	E4.8	679.22
180.75	B4.C	526.59	192.75	C0.C	564.95	204.75	CC.C	603.31	216.75	D8.C	641.66	228.75	E4.C	680.02
181.00	B5.0	527.39	193.00	C1.0	565.75	205.00	CD.0	604.10	217.00	D9.0	642.46	229.00	E5.0	680.82
181.25	B5.4	528.19	193.25	C1.4	566.55	205.25	CD.4	604.90	217.25	D9.4	643.26	229.25	E5.4	681.62
181.50	B5.8	528.99	193.50	C1.8	567.35	205.50	CD.8	605.70	217.50	D9.8	644.06	229.50	E5.8	682.42
181.75	B5.C	529.79	193.75	C1.C	568.15	205.75	CD.C	606.50	217.75	D9.C	644.86	229.75	E5.C	683.21
182.00	B6.0	530.59	194.00	C2.0	568.94	206.00	CE.0	607.30	218.00	DA.0	645.66	230.00	E6.0	684.01
182.25	B6.4	531.39	194.25	C2.4	569.74	206.25	CE.4	608.10	218.25	DA.4	646.46	230.25	E6.4	684.81
182.50	B6.8	532.19	194.50	C2.8	570.54	206.50	CE.8	608.90	218.50	DA.8	647.26	230.50	E6.8	685.61
182.75	B6.C	532.99	194.75	C2.C	571.34	206.75	CE.C	609.70	218.75	DA.C	648.05	230.75	E6.C	686.41
183.00	B7.0	533.79	195.00	C3.0	572.14	207.00	CF.0	610.50	219.00	DB.0	648.85	231.00	E7.0	687.21
183.25	B7.4	534.58	195.25	C3.4	572.94	207.25	CF.4	611.30	219.25	DB.4	649.65	231.25	E7.4	688.01
183.50	B7.8	535.38	195.50	C3.8	573.74	207.50	CF.8	612.10	219.50	DB.8	650.45	231.50	E7.8	688.81
183.75	B7.C	536.18	195.75	C3.C	574.54	207.75	CF.C	612.89	219.75	DB.C	651.25	231.75	E7.C	689.61
184.00	B8.0	536.98	196.00	C4.0	575.34	208.00	D0.0	613.69	220.00	DC.0	652.05	232.00	E8.0	690.41
184.25	B8.4	537.78	196.25	C4.4	576.14	208.25	D0.4	614.49	220.25	DC.4	652.85	232.25	E8.4	691.21
184.50	B8.8	538.58	196.50	C4.8	576.94	208.50	D0.8	615.29	220.50	DC.8	653.65	232.50	E8.8	692.00
184.75	B8.C	539.38	196.75	C4.C	577.73	208.75	D0.C	616.09	220.75	DC.C	654.45	232.75	E8.C	692.80
185.00	B9.0	540.18	197.00	C5.0	578.53	209.00	D1.0	616.89	221.00	DD.0	655.25	233.00	E9.0	693.60
185.25	B9.4	540.98	197.25	C5.4	579.33	209.25	D1.4	617.69	221.25	DD.4	656.05	233.25	E9.4	694.40
185.50	B9.8	541.78	197.50	C5.8	580.13	209.50	D1.8	618.49	221.50	DD.8	656.84	233.50	E9.8	695.20
185.75	B9.C	542.58	197.75	C5.C	580.93	209.75	D1.C	619.29	221.75	DD.C	657.64	233.75	E9.C	696.00
186.00	BA.0	543.37	198.00	C6.0	581.73	210.00	D2.0	620.09	222.00	DE.0	658.44	234.00	EA.0	696.80
186.25	BA.4	544.17	198.25	C6.4	582.53	210.25	D2.4	620.89	222.25	DE.4	659.24	234.25	EA.4	697.60
186.50	BA.8	544.97	198.50	C6.8	583.33	210.50	D2.8	621.68	222.50	DE.8	660.04	234.50	EA.8	698.40
186.75	BA.C	545.77	198.75	C6.C	584.13	210.75	D2.C	622.48	222.75	DE.C	660.84	234.75	EA.C	699.20
187.00	BB.0	546.57	199.00	C7.0	584.93	211.00	D3.0	623.28	223.00	DF.0	661.64	235.00	EB.0	700.00
187.25	BB.4	547.37	199.25	C7.4	585.73	211.25	D3.4	624.08	223.25	DF.4	662.44	235.25	EB.4	700.79
187.50	BB.8	548.17	199.50	C7.8	586.52	211.50	D3.8	624.88	223.50	DF.8	663.24	235.50	EB.8	701.59
187.75	BB.C	548.97	199.75	C7.C	587.32	211.75	D3.C	625.68	223.75	DF.C	664.04	235.75	EB.C	702.39
188.00	BC.0	549.77	200.00	C8.0	588.12	212.00	D4.0	626.48	224.00	E0.0	664.84	236.00	EC.0	703.19
188.25	BC.4	550.57	200.25	C8.4	588.92	212.25	D4.4	627.28	224.25	E0.4	665.63	236.25	EC.4	703.99
188.50	BC.8	551.37	200.50	C8.8	589.72	212.50	D4.8	628.08	224.50	E0.8	666.43	236.50	EC.8	704.79
188.75	BC.C	552.16	200.75	C8.C	590.52	212.75	D4.C	628.88	224.75	E0.C	667.23	236.75	EC.C	705.59
189.00	BD.0	552.96	201.00	C9.0	591.32	213.00	D5.0	629.68	225.00	E1.0	668.03	237.00	ED.0	706.39
189.25	BD.4	553.76	201.25	C9.4	592.12	213.25	D5.4	630.47	225.25	E1.4	668.83	237.25	ED.4	707.19
189.50	BD.8	554.56	201.50	C9.8	592.92	213.50	D5.8	631.27	225.50	E1.8	669.63	237.50	ED.8	707.99
189.75	BD.C	555.36	201.75	C9.C	593.72	213.75	D5.C	632.07	225.75	E1.C	670.43	237.75	ED.C	708.79
190.00	BE.0	556.16	202.00	CA.0	594.52	214.00	D6.0	632.87	226.00	E2.0	671.23	238.00	EE.0	709.58
190.25	BE.4	556.96	202.25	CA.4	595.31	214.25	D6.4	633.67	226.25	E2.4	672.03	238.25	EE.4	710.38
190.50	BE.8	557.76	202.50	CA.8	596.11	214.50	D6.8	634.47	226.50	E2.8	672.83	238.50	EE.8	711.18
190.75	BE.C	558.56	202.75	CA.C	596.91	214.75	D6.C	635.27	226.75	E2.C	673.63	238.75	EE.C	711.98
191.00	BF.0	559.36	203.00	CB.0	597.71	215.00	D7.0	636.07	227.00	E3.0	674.42	239.00	EF.0	712.78
191.25	BF.4	560.15	203.25	CB.4	598.51	215.25	D7.4	636.87	227.25	E3.4	675.22	239.25	EF.4	713.58
191.50	BF.8	560.95	203.50	CB.8	599.31	215.50	D7.8	637.67	227.50	E3.8	676.02	239.50	EF.8	714.38
191.75	BF.C	561.75	203.75	CB.C	600.11	215.75	D7.C	638.47	227.75	E3.C	676.82	239.75	EF.C	715.18

Ref. 20 – 10–bit luminance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
240.00	F0.0	715.98	243.00	F3.0	725.57	246.00	F6.0	735.16	249.00	F9.0	744.74	252.00	FC.0	754.33
240.25	F0.4	716.78	243.25	F3.4	726.37	246.25	F6.4	735.95	249.25	F9.4	745.54	252.25	FC.4	755.13
240.50	F0.8	717.58	243.50	F3.8	727.16	246.50	F6.8	736.75	249.50	F9.8	746.34	252.50	FC.8	755.93
240.75	F0.C	718.37	243.75	F3.C	727.96	246.75	F6.C	737.55	249.75	F9.C	747.14	252.75	FC.C	756.73
241.00	F1.0	719.17	244.00	F4.0	728.76	247.00	F7.0	738.35	250.00	FA.0	747.94	253.00	FD.0	757.53
241.25	F1.4	719.97	244.25	F4.4	729.56	247.25	F7.4	739.15	250.25	FA.4	748.74	253.25	FD.4	758.33
241.50	F1.8	720.77	244.50	F4.8	730.36	247.50	F7.8	739.95	250.50	FA.8	749.54	253.50	FD.8	759.13
241.75	F1.C	721.57	244.75	F4.C	731.16	247.75	F7.C	740.75	250.75	FA.C	750.34	253.75	FD.C	759.93
242.00	F2.0	722.37	245.00	F5.0	731.96	248.00	F8.0	741.55	251.00	FB.0	751.14	254.00	FE.0	760.73
242.25	F2.4	723.17	245.25	F5.4	732.76	248.25	F8.4	742.35	251.25	FB.4	751.94	254.25	FE.4	761.52
242.50	F2.8	723.97	245.50	F5.8	733.56	248.50	F8.8	743.15	251.50	FB.8	752.73	254.50	FE.8	762.32
242.75	F2.C	724.77	245.75	F5.C	734.36	248.75	F8.C	743.94	251.75	FB.C	753.53	254.75	FE.C	763.12

Ref. 21 – 10–bit chrominance levels

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
			12.00	0C.0	−362.50	24.00	18.0	−325.00	36.00	24.0	−287.50	48.00	30.0	−250.00
			12.25	0C.4	−361.71	24.25	18.4	−324.21	36.25	24.4	−286.71	48.25	30.4	−249.21
			12.50	0C.8	−360.93	24.50	18.8	−323.43	36.50	24.8	−285.93	48.50	30.8	−248.43
			12.75	0C.C	−360.15	24.75	18.C	−322.65	36.75	24.C	−285.15	48.75	30.C	−247.65
1.00	01.0	−396.87	13.00	0D.0	−359.37	25.00	19.0	−321.87	37.00	25.0	−284.37	49.00	31.0	−246.87
1.25	01.4	−396.09	13.25	0D.4	−358.59	25.25	19.4	−321.09	37.25	25.4	−283.59	49.25	31.4	−246.09
1.50	01.8	−395.31	13.50	0D.8	−357.81	25.50	19.8	−320.31	37.50	25.8	−282.81	49.50	31.8	−245.31
1.75	01.C	−394.53	13.75	0D.C	−357.03	25.75	19.C	−319.53	37.75	25.C	−282.03	49.75	31.C	−244.53
2.00	02.0	−393.75	14.00	0E.0	−356.25	26.00	1A.0	−318.75	38.00	26.0	−281.25	50.00	32.0	−243.75
2.25	02.4	−392.96	14.25	0E.4	−355.46	26.25	1A.4	−317.96	38.25	26.4	−280.46	50.25	32.4	−242.96
2.50	02.8	−392.18	14.50	0E.8	−354.68	26.50	1A.8	−317.18	38.50	26.8	−279.68	50.50	32.8	−242.18
2.75	02.C	−391.40	14.75	0E.C	−353.90	26.75	1A.C	−316.40	38.75	26.C	−278.90	50.75	32.C	−241.40
3.00	03.0	−390.62	15.00	0F.0	−353.12	27.00	1B.0	−315.62	39.00	27.0	−278.12	51.00	33.0	−240.62
3.25	03.4	−389.84	15.25	0F.4	−352.34	27.25	1B.4	−314.84	39.25	27.4	−277.34	51.25	33.4	−239.84
3.50	03.8	−389.06	15.50	0F.8	−351.56	27.50	1B.8	−314.06	39.50	27.8	−276.56	51.50	33.8	−239.06
3.75	03.C	−388.28	15.75	0F.C	−350.78	27.75	1B.C	−313.28	39.75	27.C	−275.78	51.75	33.C	−238.28
4.00	04.0	−387.50	16.00	10.0	−350.00	28.00	1C.0	−312.50	40.00	28.0	−275.00	52.00	34.0	−237.50
4.25	04.4	−386.71	16.25	10.4	−349.21	28.25	1C.4	−311.71	40.25	28.4	−274.21	52.25	34.4	−236.71
4.50	04.8	−385.93	16.50	10.8	−348.43	28.50	1C.8	−310.93	40.50	28.8	−273.43	52.50	34.8	−235.93
4.75	04.C	−385.15	16.75	10.C	−347.65	28.75	1C.C	−310.15	40.75	28.C	−272.65	52.75	34.C	−235.15
5.00	05.0	−384.37	17.00	11.0	−346.87	29.00	1D.0	−309.37	41.00	29.0	−271.87	53.00	35.0	−234.37
5.25	05.4	−383.59	17.25	11.4	−346.09	29.25	1D.4	−308.59	41.25	29.4	−271.09	53.25	35.4	−233.59
5.50	05.8	−382.81	17.50	11.8	−345.31	29.50	1D.8	−307.81	41.50	29.8	−270.31	53.50	35.8	−232.81
5.75	05.C	−382.03	17.75	11.C	−344.53	29.75	1D.C	−307.03	41.75	29.C	−269.53	53.75	35.C	−232.03
6.00	06.0	−381.25	18.00	12.0	−343.75	30.00	1E.0	−306.25	42.00	2A.0	−268.75	54.00	36.0	−231.25
6.25	06.4	−380.46	18.25	12.4	−342.96	30.25	1E.4	−305.46	42.25	2A.4	−267.96	54.25	36.4	−230.46
6.50	06.8	−379.68	18.50	12.8	−342.18	30.50	1E.8	−304.68	42.50	2A.8	−267.18	54.50	36.8	−229.68
6.75	06.C	−378.90	18.75	12.C	−341.40	30.75	1E.C	−303.90	42.75	2A.C	−266.40	54.75	36.C	−228.90
7.00	07.0	−378.12	19.00	13.0	−340.62	31.00	1F.0	−303.12	43.00	2B.0	−265.62	55.00	37.0	−228.12
7.25	07.4	−377.34	19.25	13.4	−339.84	31.25	1F.4	−302.34	43.25	2B.4	−264.84	55.25	37.4	−227.34
7.50	07.8	−376.56	19.50	13.8	−339.06	31.50	1F.8	−301.56	43.50	2B.8	−264.06	55.50	37.8	−226.56
7.75	07.C	−375.78	19.75	13.C	−338.28	31.75	1F.C	−300.78	43.75	2B.C	−263.28	55.75	37.C	−225.78
8.00	08.0	−375.00	20.00	14.0	−337.50	32.00	20.0	−300.00	44.00	2C.0	−262.50	56.00	38.0	−225.00
8.25	08.4	−374.21	20.25	14.4	−336.71	32.25	20.4	−299.21	44.25	2C.4	−261.71	56.25	38.4	−224.21
8.50	08.8	−373.43	20.50	14.8	−335.93	32.50	20.8	−298.43	44.50	2C.8	−260.93	56.50	38.8	−223.43
8.75	08.C	−372.65	20.75	14.C	−335.15	32.75	20.C	−297.65	44.75	2C.C	−260.15	56.75	38.C	−222.65
9.00	09.0	−371.87	21.00	15.0	−334.37	33.00	21.0	−296.87	45.00	2D.0	−259.37	57.00	39.0	−221.87
9.25	09.4	−371.09	21.25	15.4	−333.59	33.25	21.4	−296.09	45.25	2D.4	−258.59	57.25	39.4	−221.09
9.50	09.8	−370.31	21.50	15.8	−332.81	33.50	21.8	−295.31	45.50	2D.8	−257.81	57.50	39.8	−220.31
9.75	09.C	−369.53	21.75	15.C	−332.03	33.75	21.C	−294.53	45.75	2D.C	−257.03	57.75	39.C	−219.53
10.00	0A.0	−368.75	22.00	16.0	−331.25	34.00	22.0	−293.75	46.00	2E.0	−256.25	58.00	3A.0	−218.75
10.25	0A.4	−367.96	22.25	16.4	−330.46	34.25	22.4	−292.96	46.25	2E.4	−255.46	58.25	3A.4	−217.96
10.50	0A.8	−367.18	22.50	16.8	−329.68	34.50	22.8	−292.18	46.50	2E.8	−254.68	58.50	3A.8	−217.18
10.75	0A.C	−366.40	22.75	16.C	−328.90	34.75	22.C	−291.40	46.75	2E.C	−253.90	58.75	3A.C	−216.40
11.00	0B.0	−365.62	23.00	17.0	−328.12	35.00	23.0	−290.62	47.00	2F.0	−253.12	59.00	3B.0	−215.62
11.25	0B.4	−364.84	23.25	17.4	−327.34	35.25	23.4	−289.84	47.25	2F.4	−252.34	59.25	3B.4	−214.84
11.50	0B.8	−364.06	23.50	17.8	−326.56	35.50	23.8	−289.06	47.50	2F.8	−251.56	59.50	3B.8	−214.06
11.75	0B.C	−363.28	23.75	17.C	−325.78	35.75	23.C	−288.28	47.75	2F.C	−250.78	59.75	3B.C	−213.28

Ref. 21 – 10–bit chrominance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
60.00	3C.0	−212.50	72.00	48.0	−175.00	84.00	54.0	−137.50	96.00	60.0	−100.00	108.00	6C.0	−62.500
60.25	3C.4	−211.71	72.25	48.4	−174.21	84.25	54.4	−136.71	96.25	60.4	−99.218	108.25	6C.4	−61.718
60.50	3C.8	−210.93	72.50	48.8	−173.43	84.50	54.8	−135.93	96.50	60.8	−98.437	108.50	6C.8	−60.937
60.75	3C.C	−210.15	72.75	48.C	−172.65	84.75	54.C	−135.15	96.75	60.C	−97.656	108.75	6C.C	−60.156
61.00	3D.0	−209.37	73.00	49.0	−171.87	85.00	55.0	−134.37	97.00	61.0	−96.875	109.00	6D.0	−59.375
61.25	3D.4	−208.59	73.25	49.4	−171.09	85.25	55.4	−133.59	97.25	61.4	−96.093	109.25	6D.4	−58.593
61.50	3D.8	−207.81	73.50	49.8	−170.31	85.50	55.8	−132.81	97.50	61.8	−95.312	109.50	6D.8	−57.812
61.75	3D.C	−207.03	73.75	49.C	−169.53	85.75	55.C	−132.03	97.75	61.C	−94.531	109.75	6D.C	−57.031
62.00	3E.0	−206.25	74.00	4A.0	−168.75	86.00	56.0	−131.25	98.00	62.0	−93.750	110.00	6E.0	−56.250
62.25	3E.4	−205.46	74.25	4A.4	−167.96	86.25	56.4	−130.46	98.25	62.4	−92.968	110.25	6E.4	−55.468
62.50	3E.8	−204.68	74.50	4A.8	−167.18	86.50	56.8	−129.68	98.50	62.8	−92.187	110.50	6E.8	−54.687
62.75	3E.C	−203.90	74.75	4A.C	−166.40	86.75	56.C	−128.90	98.75	62.C	−91.406	110.75	6E.C	−53.906
63.00	3F.0	−203.12	75.00	4B.0	−165.62	87.00	57.0	−128.12	99.00	63.0	−90.625	111.00	6F.0	−53.125
63.25	3F.4	−202.34	75.25	4B.4	−164.84	87.25	57.4	−127.34	99.25	63.4	−89.843	111.25	6F.4	−52.343
63.50	3F.8	−201.56	75.50	4B.8	−164.06	87.50	57.8	−126.56	99.50	63.8	−89.062	111.50	6F.8	−51.562
63.75	3F.C	−200.78	75.75	4B.C	−163.28	87.75	57.C	−125.78	99.75	63.C	−88.281	111.75	6F.C	−50.781
64.00	40.0	−200.00	76.00	4C.0	−162.50	88.00	58.0	−125.00	100.00	64.0	−87.500	112.00	70.0	−50.000
64.25	40.4	−199.21	76.25	4C.4	−161.71	88.25	58.4	−124.21	100.25	64.4	−86.718	112.25	70.4	−49.218
64.50	40.8	−198.43	76.50	4C.8	−160.93	88.50	58.8	−123.43	100.50	64.8	−85.937	112.50	70.8	−48.437
64.75	40.C	−197.65	76.75	4C.C	−160.15	88.75	58.C	−122.65	100.75	64.C	−85.156	112.75	70.C	−47.656
65.00	41.0	−196.87	77.00	4D.0	−159.37	89.00	59.0	−121.87	101.00	65.0	−84.375	113.00	71.0	−46.875
65.25	41.4	−196.09	77.25	4D.4	−158.59	89.25	59.4	−121.09	101.25	65.4	−83.593	113.25	71.4	−46.093
65.50	41.8	−195.31	77.50	4D.8	−157.81	89.50	59.8	−120.31	101.50	65.8	−82.812	113.50	71.8	−45.312
65.75	41.C	−194.53	77.75	4D.C	−157.03	89.75	59.C	−119.53	101.75	65.C	−82.031	113.75	71.C	−44.531
66.00	42.0	−193.75	78.00	4E.0	−156.25	90.00	5A.0	−118.75	102.00	66.0	−81.250	114.00	72.0	−43.750
66.25	42.4	−192.96	78.25	4E.4	−155.46	90.25	5A.4	−117.96	102.25	66.4	−80.468	114.25	72.4	−42.968
66.50	42.8	−192.18	78.50	4E.8	−154.68	90.50	5A.8	−117.18	102.50	66.8	−79.687	114.50	72.8	−42.187
66.75	42.C	−191.40	78.75	4E.C	−153.90	90.75	5A.C	−116.40	102.75	66.C	−78.906	114.75	72.C	−41.406
67.00	43.0	−190.62	79.00	4F.0	−153.12	91.00	5B.0	−115.62	103.00	67.0	−78.125	115.00	73.0	−40.625
67.25	43.4	−189.84	79.25	4F.4	−152.34	91.25	5B.4	−114.84	103.25	67.4	−77.343	115.25	73.4	−39.843
67.50	43.8	−189.06	79.50	4F.8	−151.56	91.50	5B.8	−114.06	103.50	67.8	−76.562	115.50	73.8	−39.062
67.75	43.C	−188.28	79.75	4F.C	−150.78	91.75	5B.C	−113.28	103.75	67.C	−75.781	115.75	73.C	−38.281
68.00	44.0	−187.50	80.00	50.0	−150.00	92.00	5C.0	−112.50	104.00	68.0	−75.000	116.00	74.0	−37.500
68.25	44.4	−186.71	80.25	50.4	−149.21	92.25	5C.4	−111.71	104.25	68.4	−74.218	116.25	74.4	−36.718
68.50	44.8	−185.93	80.50	50.8	−148.43	92.50	5C.8	−110.93	104.50	68.8	−73.437	116.50	74.8	−35.937
68.75	44.C	−185.15	80.75	50.C	−147.65	92.75	5C.C	−110.15	104.75	68.C	−72.656	116.75	74.C	−35.156
69.00	45.0	−184.37	81.00	51.0	−146.87	93.00	5D.0	−109.37	105.00	69.0	−71.875	117.00	75.0	−34.375
69.25	45.4	−183.59	81.25	51.4	−146.09	93.25	5D.4	−108.59	105.25	69.4	−71.093	117.25	75.4	−33.593
69.50	45.8	−182.81	81.50	51.8	−145.31	93.50	5D.8	−107.81	105.50	69.8	−70.312	117.50	75.8	−32.812
69.75	45.C	−182.03	81.75	51.C	−144.53	93.75	5D.C	−107.03	105.75	69.C	−69.531	117.75	75.C	−32.031
70.00	46.0	−181.25	82.00	52.0	−143.75	94.00	5E.0	−106.25	106.00	6A.0	−68.750	118.00	76.0	−31.250
70.25	46.4	−180.46	82.25	52.4	−142.96	94.25	5E.4	−105.46	106.25	6A.4	−67.968	118.25	76.4	−30.468
70.50	46.8	−179.68	82.50	52.8	−142.18	94.50	5E.8	−104.68	106.50	6A.8	−67.187	118.50	76.8	−29.687
70.75	46.C	−178.90	82.75	52.C	−141.40	94.75	5E.C	−103.90	106.75	6A.C	−66.406	118.75	76.C	−28.906
71.00	47.0	−178.12	83.00	53.0	−140.62	95.00	5F.0	−103.12	107.00	6B.0	−65.625	119.00	77.0	−28.125
71.25	47.4	−177.34	83.25	53.4	−139.84	95.25	5F.4	−102.34	107.25	6B.4	−64.843	119.25	77.4	−27.343
71.50	47.8	−176.56	83.50	53.8	−139.06	95.50	5F.8	−101.56	107.50	6B.8	−64.062	119.50	77.8	−26.562
71.75	47.C	−175.78	83.75	53.C	−138.28	95.75	5F.C	−100.78	107.75	6B.C	−63.281	119.75	77.C	−25.781

Ref. 21 – 10–bit chrominance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
120.00	78.0	−25.000	132.00	84.0	12.500	144.00	90.0	50.000	156.00	9C.0	87.500	168.00	A8.0	125.00
120.25	78.4	−24.218	132.25	84.4	13.281	144.25	90.4	50.781	156.25	9C.4	88.281	168.25	A8.4	125.78
120.50	78.8	−23.437	132.50	84.8	14.062	144.50	90.8	51.562	156.50	9C.8	89.062	168.50	A8.8	126.56
120.75	78.C	−22.656	132.75	84.C	14.843	144.75	90.C	52.343	156.75	9C.C	89.843	168.75	A8.C	127.34
121.00	79.0	−21.875	133.00	85.0	15.625	145.00	91.0	53.125	157.00	9D.0	90.625	169.00	A9.0	128.12
121.25	79.4	−21.093	133.25	85.4	16.406	145.25	91.4	53.906	157.25	9D.4	91.406	169.25	A9.4	128.90
121.50	79.8	−20.312	133.50	85.8	17.187	145.50	91.8	54.687	157.50	9D.8	92.187	169.50	A9.8	129.68
121.75	79.C	−19.531	133.75	85.C	17.968	145.75	91.C	55.468	157.75	9D.C	92.968	169.75	A9.C	130.46
122.00	7A.0	−18.750	134.00	86.0	18.750	146.00	92.0	56.250	158.00	9E.0	93.750	170.00	AA.0	131.25
122.25	7A.4	−17.968	134.25	86.4	19.531	146.25	92.4	57.031	158.25	9E.4	94.531	170.25	AA.4	132.03
122.50	7A.8	−17.187	134.50	86.8	20.312	146.50	92.8	57.812	158.50	9E.8	95.312	170.50	AA.8	132.81
122.75	7A.C	−16.406	134.75	86.C	21.093	146.75	92.C	58.593	158.75	9E.C	96.093	170.75	AA.C	133.59
123.00	7B.0	−15.625	135.00	87.0	21.875	147.00	93.0	59.375	159.00	9F.0	96.875	171.00	AB.0	134.37
123.25	7B.4	−14.843	135.25	87.4	22.656	147.25	93.4	60.156	159.25	9F.4	97.656	171.25	AB.4	135.15
123.50	7B.8	−14.062	135.50	87.8	23.437	147.50	93.8	60.937	159.50	9F.8	98.437	171.50	AB.8	135.93
123.75	7B.C	−13.281	135.75	87.C	24.218	147.75	93.C	61.718	159.75	9F.C	99.218	171.75	AB.C	136.71
124.00	7C.0	−12.500	136.00	88.0	25.000	148.00	94.0	62.500	160.00	A0.0	100.00	172.00	AC.0	137.50
124.25	7C.4	−11.718	136.25	88.4	25.781	148.25	94.4	63.281	160.25	A0.4	100.78	172.25	AC.4	138.28
124.50	7C.8	−10.937	136.50	88.8	26.562	148.50	94.8	64.062	160.50	A0.8	101.56	172.50	AC.8	139.06
124.75	7C.C	−10.156	136.75	88.C	27.343	148.75	94.C	64.843	160.75	A0.C	102.34	172.75	AC.C	139.84
125.00	7D.0	−9.3750	137.00	89.0	28.125	149.00	95.0	65.625	161.00	A1.0	103.12	173.00	AD.0	140.62
125.25	7D.4	−8.5937	137.25	89.4	28.906	149.25	95.4	66.406	161.25	A1.4	103.90	173.25	AD.4	141.40
125.50	7D.8	−7.8125	137.50	89.8	29.687	149.50	95.8	67.187	161.50	A1.8	104.68	173.50	AD.8	142.18
125.75	7D.C	−7.0312	137.75	89.C	30.468	149.75	95.C	67.968	161.75	A1.C	105.46	173.75	AD.C	142.96
126.00	7E.0	−6.2500	138.00	8A.0	31.250	150.00	96.0	68.750	162.00	A2.0	106.25	174.00	AE.0	143.75
126.25	7E.4	−5.4687	138.25	8A.4	32.031	150.25	96.4	69.531	162.25	A2.4	107.03	174.25	AE.4	144.53
126.50	7E.8	−4.6875	138.50	8A.8	32.812	150.50	96.8	70.312	162.50	A2.8	107.81	174.50	AE.8	145.31
126.75	7E.C	−3.9062	138.75	8A.C	33.593	150.75	96.C	71.093	162.75	A2.C	108.59	174.75	AE.C	146.09
127.00	7F.0	−3.1250	139.00	8B.0	34.375	151.00	97.0	71.875	163.00	A3.0	109.37	175.00	AF.0	146.87
127.25	7F.4	−2.3437	139.25	8B.4	35.156	151.25	97.4	72.656	163.25	A3.4	110.15	175.25	AF.4	147.65
127.50	7F.8	−1.5625	139.50	8B.8	35.937	151.50	97.8	73.437	163.50	A3.8	110.93	175.50	AF.8	148.43
127.75	7F.C	−.78125	139.75	8B.C	36.718	151.75	97.C	74.218	163.75	A3.C	111.71	175.75	AF.C	149.21
128.00	80.0	0	140.00	8C.0	37.500	152.00	98.0	75.000	164.00	A4.0	112.50	176.00	B0.0	150.00
128.25	80.4	0.78125	140.25	8C.4	38.281	152.25	98.4	75.781	164.25	A4.4	113.28	176.25	B0.4	150.78
128.50	80.8	1.5625	140.50	8C.8	39.062	152.50	98.8	76.562	164.50	A4.8	114.06	176.50	B0.8	151.56
128.75	80.C	2.3437	140.75	8C.C	39.843	152.75	98.C	77.343	164.75	A4.C	114.84	176.75	B0.C	152.34
129.00	81.0	3.1250	141.00	8D.0	40.625	153.00	99.0	78.125	165.00	A5.0	115.62	177.00	B1.0	153.12
129.25	81.4	3.9062	141.25	8D.4	41.406	153.25	99.4	78.906	165.25	A5.4	116.40	177.25	B1.4	153.90
129.50	81.8	4.6875	141.50	8D.8	42.187	153.50	99.8	79.687	165.50	A5.8	117.18	177.50	B1.8	154.68
129.75	81.C	5.4687	141.75	8D.C	42.968	153.75	99.C	80.468	165.75	A5.C	117.96	177.75	B1.C	155.46
130.00	82.0	6.2500	142.00	8E.0	43.750	154.00	9A.0	81.250	166.00	A6.0	118.75	178.00	B2.0	156.25
130.25	82.4	7.0312	142.25	8E.4	44.531	154.25	9A.4	82.031	166.25	A6.4	119.53	178.25	B2.4	157.03
130.50	82.8	7.8125	142.50	8E.8	45.312	154.50	9A.8	82.812	166.50	A6.8	120.31	178.50	B2.8	157.81
130.75	82.C	8.5937	142.75	8E.C	46.093	154.75	9A.C	83.593	166.75	A6.C	121.09	178.75	B2.C	158.59
131.00	83.0	9.3750	143.00	8F.0	46.875	155.00	9B.0	84.375	167.00	A7.0	121.87	179.00	B3.0	159.37
131.25	83.4	10.156	143.25	8F.4	47.656	155.25	9B.4	85.156	167.25	A7.4	122.65	179.25	B3.4	160.15
131.50	83.8	10.937	143.50	8F.8	48.437	155.50	9B.8	85.937	167.50	A7.8	123.43	179.50	B3.8	160.93
131.75	83.C	11.718	143.75	8F.C	49.218	155.75	9B.C	86.718	167.75	A7.C	124.21	179.75	B3.C	161.71

Ref. 21 – 10–bit chrominance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
180.00	B4.0	162.50	192.00	C0.0	200.00	204.00	CC.0	237.50	216.00	D8.0	275.00	228.00	E4.0	312.50
180.25	B4.4	163.28	192.25	C0.4	200.78	204.25	CC.4	238.28	216.25	D8.4	275.78	228.25	E4.4	313.28
180.50	B4.8	164.06	192.50	C0.8	201.56	204.50	CC.8	239.06	216.50	D8.8	276.56	228.50	E4.8	314.06
180.75	B4.C	164.84	192.75	C0.C	202.34	204.75	CC.C	239.84	216.75	D8.C	277.34	228.75	E4.C	314.84
181.00	B5.0	165.62	193.00	C1.0	203.12	205.00	CD.0	240.62	217.00	D9.0	278.12	229.00	E5.0	315.62
181.25	B5.4	166.40	193.25	C1.4	203.90	205.25	CD.4	241.40	217.25	D9.4	278.90	229.25	E5.4	316.40
181.50	B5.8	167.18	193.50	C1.8	204.68	205.50	CD.8	242.18	217.50	D9.8	279.68	229.50	E5.8	317.18
181.75	B5.C	167.96	193.75	C1.C	205.46	205.75	CD.C	242.96	217.75	D9.C	280.46	229.75	E5.C	317.96
182.00	B6.0	168.75	194.00	C2.0	206.25	206.00	CE.0	243.75	218.00	DA.0	281.25	230.00	E6.0	318.75
182.25	B6.4	169.53	194.25	C2.4	207.03	206.25	CE.4	244.53	218.25	DA.4	282.03	230.25	E6.4	319.53
182.50	B6.8	170.31	194.50	C2.8	207.81	206.50	CE.8	245.31	218.50	DA.8	282.81	230.50	E6.8	320.31
182.75	B6.C	171.09	194.75	C2.C	208.59	206.75	CE.C	246.09	218.75	DA.C	283.59	230.75	E6.C	321.09
183.00	B7.0	171.87	195.00	C3.0	209.37	207.00	CF.0	246.87	219.00	DB.0	284.37	231.00	E7.0	321.87
183.25	B7.4	172.65	195.25	C3.4	210.15	207.25	CF.4	247.65	219.25	DB.4	285.15	231.25	E7.4	322.65
183.50	B7.8	173.43	195.50	C3.8	210.93	207.50	CF.8	248.43	219.50	DB.8	285.93	231.50	E7.8	323.43
183.75	B7.C	174.21	195.75	C3.C	211.71	207.75	CF.C	249.21	219.75	DB.C	286.71	231.75	E7.C	324.21
184.00	B8.0	175.00	196.00	C4.0	212.50	208.00	D0.0	250.00	220.00	DC.0	287.50	232.00	E8.0	325.00
184.25	B8.4	175.78	196.25	C4.4	213.28	208.25	D0.4	250.78	220.25	DC.4	288.28	232.25	E8.4	325.78
184.50	B8.8	176.56	196.50	C4.8	214.06	208.50	D0.8	251.56	220.50	DC.8	289.06	232.50	E8.8	326.56
184.75	B8.C	177.34	196.75	C4.C	214.84	208.75	D0.C	252.34	220.75	DC.C	289.84	232.75	E8.C	327.34
185.00	B9.0	178.12	197.00	C5.0	215.62	209.00	D1.0	253.12	221.00	DD.0	290.62	233.00	E9.0	328.12
185.25	B9.4	178.90	197.25	C5.4	216.40	209.25	D1.4	253.90	221.25	DD.4	291.40	233.25	E9.4	328.90
185.50	B9.8	179.68	197.50	C5.8	217.18	209.50	D1.8	254.68	221.50	DD.8	292.18	233.50	E9.8	329.68
185.75	B9.C	180.46	197.75	C5.C	217.96	209.75	D1.C	255.46	221.75	DD.C	292.96	233.75	E9.C	330.46
186.00	BA.0	181.25	198.00	C6.0	218.75	210.00	D2.0	256.25	222.00	DE.0	293.75	234.00	EA.0	331.25
186.25	BA.4	182.03	198.25	C6.4	219.53	210.25	D2.4	257.03	222.25	DE.4	294.53	234.25	EA.4	332.03
186.50	BA.8	182.81	198.50	C6.8	220.31	210.50	D2.8	257.81	222.50	DE.8	295.31	234.50	EA.8	332.81
186.75	BA.C	183.59	198.75	C6.C	221.09	210.75	D2.C	258.59	222.75	DE.C	296.09	234.75	EA.C	333.59
187.00	BB.0	184.37	199.00	C7.0	221.87	211.00	D3.0	259.37	223.00	DF.0	296.87	235.00	EB.0	334.37
187.25	BB.4	185.15	199.25	C7.4	222.65	211.25	D3.4	260.15	223.25	DF.4	297.65	235.25	EB.4	335.15
187.50	BB.8	185.93	199.50	C7.8	223.43	211.50	D3.8	260.93	223.50	DF.8	298.43	235.50	EB.8	335.93
187.75	BB.C	186.71	199.75	C7.C	224.21	211.75	D3.C	261.71	223.75	DF.C	299.21	235.75	EB.C	336.71
188.00	BC.0	187.50	200.00	C8.0	225.00	212.00	D4.0	262.50	224.00	E0.0	300.00	236.00	EC.0	337.50
188.25	BC.4	188.28	200.25	C8.4	225.78	212.25	D4.4	263.28	224.25	E0.4	300.78	236.25	EC.4	338.28
188.50	BC.8	189.06	200.50	C8.8	226.56	212.50	D4.8	264.06	224.50	E0.8	301.56	236.50	EC.8	339.06
188.75	BC.C	189.84	200.75	C8.C	227.34	212.75	D4.C	264.84	224.75	E0.C	302.34	236.75	EC.C	339.84
189.00	BD.0	190.62	201.00	C9.0	228.12	213.00	D5.0	265.62	225.00	E1.0	303.12	237.00	ED.0	340.62
189.25	BD.4	191.40	201.25	C9.4	228.90	213.25	D5.4	266.40	225.25	E1.4	303.90	237.25	ED.4	341.40
189.50	BD.8	192.18	201.50	C9.8	229.68	213.50	D5.8	267.18	225.50	E1.8	304.68	237.50	ED.8	342.18
189.75	BD.C	192.96	201.75	C9.C	230.46	213.75	D5.C	267.96	225.75	E1.C	305.46	237.75	ED.C	342.96
190.00	BE.0	193.75	202.00	CA.0	231.25	214.00	D6.0	268.75	226.00	E2.0	306.25	238.00	EE.0	343.75
190.25	BE.4	194.53	202.25	CA.4	232.03	214.25	D6.4	269.53	226.25	E2.4	307.03	238.25	EE.4	344.53
190.50	BE.8	195.31	202.50	CA.8	232.81	214.50	D6.8	270.31	226.50	E2.8	307.81	238.50	EE.8	345.31
190.75	BE.C	196.09	202.75	CA.C	233.59	214.75	D6.C	271.09	226.75	E2.C	308.59	238.75	EE.C	346.09
191.00	BF.0	196.87	203.00	CB.0	234.37	215.00	D7.0	271.87	227.00	E3.0	309.37	239.00	EF.0	346.87
191.25	BF.4	197.65	203.25	CB.4	235.15	215.25	D7.4	272.65	227.25	E3.4	310.15	239.25	EF.4	347.65
191.50	BF.8	198.43	203.50	CB.8	235.93	215.50	D7.8	273.43	227.50	E3.8	310.93	239.50	EF.8	348.43
191.75	BF.C	199.21	203.75	CB.C	236.71	215.75	D7.C	274.21	227.75	E3.C	311.71	239.75	EF.C	349.21

Ref. 21 – 10–bit chrominance levels (contd.)

step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV	step	hex	mV
240.00	F0.0	350.00	243.00	F3.0	359.37	246.00	F6.0	368.75	249.00	F9.0	378.12	252.00	FC.0	387.50
240.25	F0.4	350.78	243.25	F3.4	360.15	246.25	F6.4	369.53	249.25	F9.4	378.90	252.25	FC.4	388.28
240.50	F0.8	351.56	243.50	F3.8	360.93	246.50	F6.8	370.31	249.50	F9.8	379.68	252.50	FC.8	389.06
240.75	F0.C	352.34	243.75	F3.C	361.71	246.75	F6.C	371.09	249.75	F9.C	380.46	252.75	FC.C	389.84
241.00	F1.0	353.12	244.00	F4.0	362.50	247.00	F7.0	371.87	250.00	FA.0	381.25	253.00	FD.0	390.62
241.25	F1.4	353.90	244.25	F4.4	363.28	247.25	F7.4	372.65	250.25	FA.4	382.03	253.25	FD.4	391.40
241.50	F1.8	354.68	244.50	F4.8	364.06	247.50	F7.8	373.43	250.50	FA.8	382.81	253.50	FD.8	392.18
241.75	F1.C	355.46	244.75	F4.C	364.84	247.75	F7.C	374.21	250.75	FA.C	383.59	253.75	FD.C	392.96
242.00	F2.0	356.25	245.00	F5.0	365.62	248.00	F8.0	375.00	251.00	FB.0	384.37	254.00	FE.0	393.75
242.25	F2.4	357.03	245.25	F5.4	366.40	248.25	F8.4	375.78	251.25	FB.4	385.15	254.25	FE.4	394.53
242.50	F2.8	357.81	245.50	F5.8	367.18	248.50	F8.8	376.56	251.50	FB.8	385.93	254.50	FE.8	395.31
242.75	F2.C	358.59	245.75	F5.C	367.96	248.75	F8.C	377.34	251.75	FB.C	386.71	254.75	FE.C	396.09

Standards and specifications

This Section lists the formal standards documents covering each interface discussed in this document. The version numbers and/or dates of issue were the most–recent ones known at the time of going to press; users should check that they are using the most appropriate version for the equipment or systems under test at any time.

Digital video standards (4:2:2 and 4:4:4)

[S.1] ITU–R Recommendation BT.601–3: *Encoding parameters of digital television for studios.*

[S.2] EBU Technical Statement D72–1992: *Digital production standard for 16:9 television programmes*

[S.3] EBU document Tech. 3267 (2nd edition, 1992): *EBU interfaces for 625–line digital video signals at the 4:2:2 level of CCIR Recommendation 601*

[S.4] EBU document Tech. 3268 (2nd edition, 1992): *EBU interfaces for 625–line digital video signals at the 4:4:4 level of CCIR Recommendation 601*

[S.5] ITU–R Recommendation BT.656–1: *Interfaces for digital component video signals in 525–line and 625–line television systems operating at the 4:2:2 level of Recommendation 601.*

[S.6] SMPTE Standard 259M (January 1995): *SMPTE Standard for television – 10–bit 4:2:2 component and* $4f_{sc}$ *PAL digital signals, serial digital interface*

[S.7] SMPTE Standard 125M (December 1994): *SMPTE Standard for television – Component video signal 4:2:2 – Bit–parallel digital interface*

[S.8] SMPTE Standard 244M (September 1994): *SMPTE Standard for television – System M/NTSC, PAL video signals – Bit–parallel interface*

[S.9] SMPTE Standard 291M (JUanuary 1996): *SMPTE Standard for television – Ancillary data packet and space formatting*

[S.10] Proposed SMPTE Standard 297M (May 1996): *SMPTE Standard for television – Serial digital fibre transmission system for ANSI/SMPTE 259M signals*

Other digital video standards

[S.11] SMPTE Standard 240M (1995): *SMPTE Standard for television – Signal parameters – 1125–line high–definition production systems*

[S.12] SMPTE Standard 260M (1992): *SMPTE Standard for television – Digital representation and bit–parallel interface – 1125/60 high–definition production system*

[S.13] CCIR Recommendation 721: *Transmission of component–coded digital television signals for contribution–quality applications at bit–rates near 140 Mbit/s*

[S.14] CCIR Recommendation 723: *Transmission of component–coded digital television signals for contribution–quality applications at the third hierarchical level of CCITT Recommendation G.702*

[S.15] European Telecommunication Standard ETS 300 174: *Network aspects: Digital coding of component television signals for contribution quality applications in the range 34–45 Mbit/s*

[S.16] ITU–R Recommendation BT.709–1: *Basic parameter values for the HDTV standard for the studio and for international programme exchange.*

[S.17] ISO/IEC IS 13818–1 (1995): Coding of moving pictures and associated audio – Part 1: “Systems”
ISO/IEC IS 13818–1 (1995): Coding of moving pictures and associated audio – Part 2: “Video”
ISO/IEC IS 13818–1 (1995): Coding of moving pictures and associated audio – Part 3: “Audio”

[S.18] EBU document Tech. 3280 (1995): *Specification of interfaces for 625–line digital PAL signals*

[S.19] European Telecommunication Standard ETS 300 294: *Television systems; 625–line television: Wide Screen Signalling (WSS)*

Analogue video standards

[S.20] EBU Technical Standard N10–1989: *Parallel interface for analogue component video signals*

Synchronization, timing

[S.21] EBU Technical Standard N14–1988: *Specification of a reference signal for the synchronization of 625–line component digital equipment*

[S.22] ITU–R Recommendation BT.711–1: *Synchronizing reference signals for the component digital studio.* (See also draft revision in ITU document 11/BL/39 – May 1992)

[S.23] EBU Technical Recommendation R37–1986: *The relative timing of the sound and vision components of a television signal*

[S.24] SMPTE Recommended Practice 168 (April 1993): *Definition of vertical interval switching point for synchronous video switching*

[S.25] SMPTE Recommended Practice RP187 (1995): *Center, aspect ratio and blanking of video images*

Digital audio standards (including integration within digital video signals)

[S.26] EBU document Tech. 3250 (2nd edition, 1992): *Specification of the digital audio interface (The AES/EBU interface)*

[S.27] EBU document Tech. 3250, Supplement 1 (1992): *Format for the user data channel*

[S.28] EBU Technical Recommendation R69: *Format for ancillary data with digital audio signals*

[S.29] AES 3–1992: *AES Recommended Practice for digital audio engineering – Serial transmission format for two–channel linearly represented digital audio data*

[S.30] ITU–R Recommendation BS.647–2: *A digital audio interface for broadcasting studios.*

[S.31] IEC Publication 958: *Digital audio interface*

[S.32] SMPTE Recommended Practice 272M (April 1994): *Proposed SMPTE standard for television – Formatting AES/EBU audio and auxiliary data into digital video ancillary data space*

Test signals, measurement, diagnostics, error processing

[S.33] ITU–R Recommendation BT.801: *Test signals for digitally encoded colour television signals conforming with Recommendations 601 and 656.*

[S.34] ARD/ZDF Messrichtlinien Pflichtenheft 8/1.1,, Kap. 1.14 (April 1995): *Messtechnik für digitale Videosignale* (Measurement guidelines for serial digital television)

[S.35] SMPTE Recommended Practice 178 (April 1996): *Serial digital interface check field for 10–bit 4:2:2 component and* $4f_{sc}$ *composite digital signals*

[S.36] EBU Technical Information I15–1989: *Testing for conformity with ITU–R Recommendations BT.601 and BT.656*

[S.37] SMPTE Recommended Practice 184 (1995): *Measurement of jitter in bit–serial digital interfaces*

[S.38] SMPTE Standard 273M (1995): *SMPTE Standard for television – Status, monitoring and diagnostic protocol*

[S.39] SMPTE Recommended Practice 165 (July 1994): *Error detection check words and status flags for use in bit serial digital interfaces for television*

[S.40] SMPTE Standard 269M (October 1993): *SMPTE standard for television – Fault reporting in television systems*

[S.41] AES 11–1991: *AES Recommended Practice for digital audio engineering – Synchronization of digital audio equipment in studio operations*

[S.42] AES 17–1991: *AES Standard method for digital audio engineering – Measurement of audio equipment*

Digital television recording standards

D1 format

[S.43] IEC Publication 1016: *Helical–scan digital component video cassette recording system using 19–mm magnetic tape (format D–1)*

[S.44] ITU–R Recommendation BT.657: *Digital television tape recording. Standards for the international exchange of television programmes on magnetic tape.*

[S.45] SMPTE Recommended Practice 181 (April 1994): *Audio sector time code and equipment type information for 19–mm Type D–1 digital component recording*

D2 format

[S.46] IEC Publication 1079: *Helical–scan digital composite video cassette recording system using 19–mm magnetic tape, format D–2 (NTSC, PAL, PAL–M)*

[S.47] SMPTE Recommended Practice 245M (December 1993): *SMPTE Standard for television digital recording – 19–mm Type D–2 PAL format – Tape record*

[S.48] SMPTE Recommended Practice 246M (August 1993): *SMPTE Standard for television digital recording – 19–mm Type D–2 PAL format – Magnetic tape*

[S.49] SMPTE Recommended Practice 247M (December 1993): *SMPTE Standard for television digital recording – 19–mm Type D–2 PAL format – Helical data and control records*

[S.50] SMPTE Recommended Practice 248M (August 1993): *SMPTE Standard for television digital recording – 19–mm Type D–2 PAL format – Cue record and time and control code record*

D3 format

[S.51] SMPTE Recommended Practice 263M (June 1993): *SMPTE Standard for television digital recording – 1/2–in. Type D–3 PAL format – Tape cassette*

[S.52] SMPTE Recommended Practice 264M (June 1993): *SMPTE Standard for television digital recording – 1/2–in. Type D–3 PAL format – 525/60*

D5 format

[S.53] SMPTE Standard 279M (May 1995): *SMPTE Standard for digital television recording – 1/2–in Type D–5 component format – 525/60 and 625/50*

Appendix A

Jitter in the serial digital interface

The measurement of jitter in the serial digital interface (SDI) at 270 Mbit/s is probably the most difficult measurement in any area of television interface technology.

This Appendix discusses the terminology used to discuss jitter phenomena, techniques used to remove jitter, and the impact of jitter on digital system performance.

A1. Definitions of jitter and related concepts

In an ideal digital transmission system, individual bits of a data–stream would have exactly the same phase as the corresponding clock signal. In any real system, the data bits incoming to the data receiver differ in their relationship to the clock. This undesirable pulse–position modulation is called "jitter".

Jitter is quantified in terms of its frequency and amplitude.

A1.1. Jitter frequency

It is convenient to classify jitter frequencies according to their spectral position relative to the characteristics of filters in SDI equipment. *Fig. A1* shows idealized filter responses for jitter measurement and the corresponding transfer functions of a clock extractor, discussed in *Section A5.1*.

a) Wander

Wander is the term used to describe all jitter at frequencies of less than 10 Hz (below *B1* in *Fig. A1*). This form of jitter is not considered in the present document[7].

b) Timing jitter (absolute jitter)

Timing jitter is defined as the variation in time of the significant instants of a digital signal, *relative to the related reference clock, for variations occurring at a frequency greater than 10 Hz.*

c) Alignment jitter (relative jitter)

Alignment jitter is defined as the variation in time of the significant instants of a digital signal, *relative to the related recovered clock.*

d) Absolute or "all–frequency" jitter (including wander)

Absolute jitter is defined as the variation in time of the significant instants of a digital signal, *relative to the related reference clock.*

7. However, the jitter measurement technique discussed in *Section 4.2.5., Method 4*, will include the effects of wander.

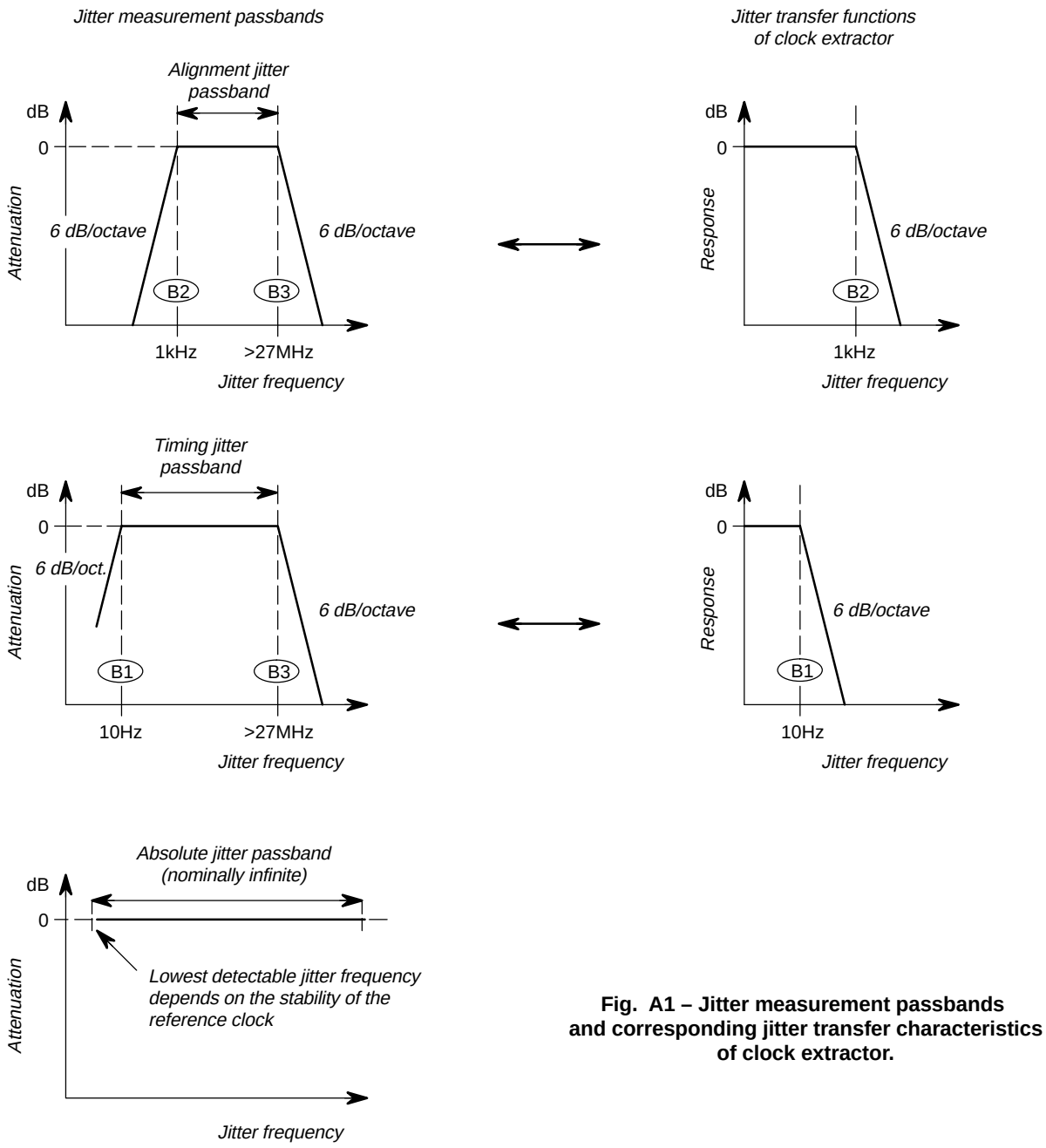


Fig. A1 – Jitter measurement passbands and corresponding jitter transfer characteristics of clock extractor.

A1.2. Jitter amplitude

Jitter amplitude is conveniently quantified in terms of “unit intervals” (UI). One UI is the nominal duration of one clock period. In the 270 MHz domain, 1 UI corresponds to a duration of 3.7 ns.

An advantage of this unit of measurement is that, for a number of bit–rates, a given jitter amplitude, expressed in UI, will be independent of the data–rate.

A1.3. Jitter transfer function

In a device which produces a serial output from a serial input, the jitter transfer function is the ratio of the output jitter to the applied input jitter. It is measured as a function of frequency.

Fig. A2 shows an imaginary jitter transfer function of a phase–locked loop (PLL) data regenerator with critical overshoot. In the overshoot range, the jitter amplitude of the incoming signal will be increased. If a number of PLL devices with identical clock–recovery characteristics are cascaded, the jitter in the overshoot range will be accumulated proportionately to the number of cascaded regenerators.

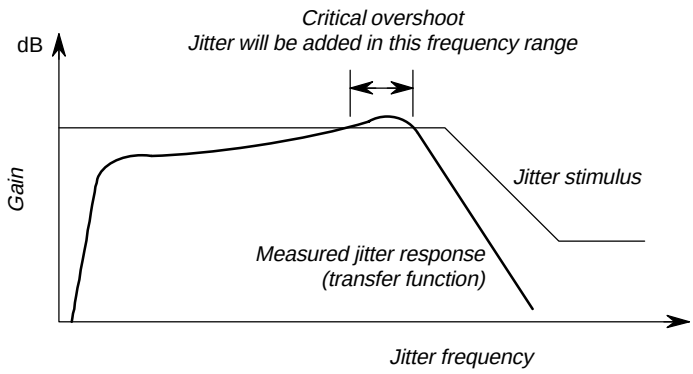


Fig. A2 – Jitter transfer function of a data regenerator with critical overshoot.

A2. Jitter removal

For some applications, and especially at the input to digital–to–analogue converters (DAC), jitter should be maintained below 1 ns for video signals and 0.1 ns for 16–bit audio. Jitter which exceeds these limits can lead to linearity and other errors in the analogue domain [2][3].

A jitter remover is a device which takes an SDI signal suffering from jitter and delivers at its output a signal which is highly stable and almost jitter–free. A block diagram of the process is shown in *Fig. A3*. It consists basically of two phase–locked loops (PLL) and a first–in/first–out (FIFO) buffer.

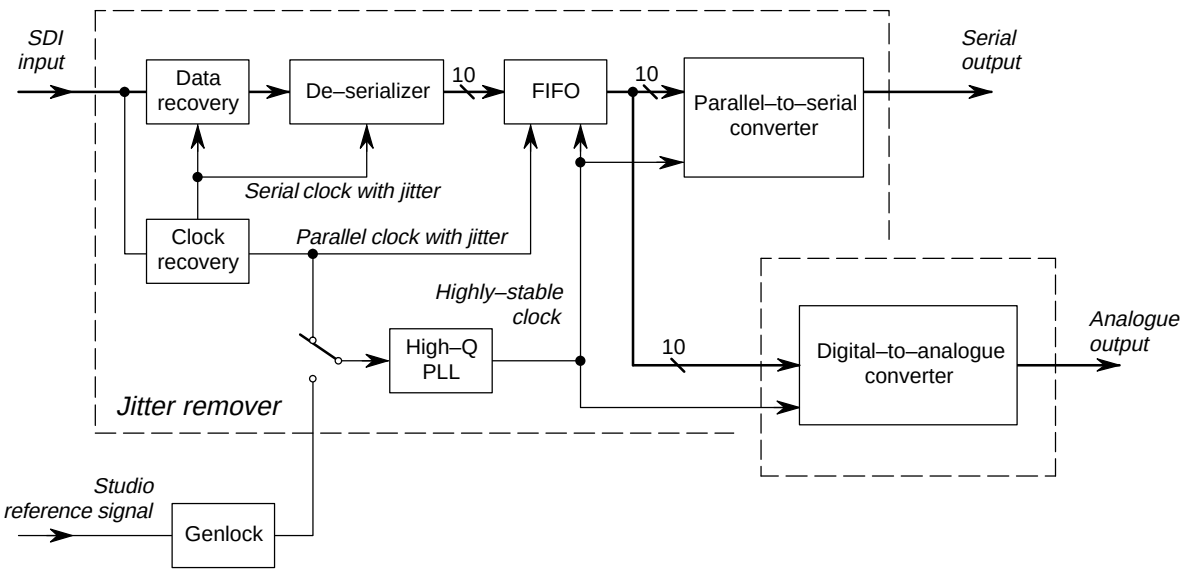


Fig. A3 – Block diagram of a jitter remover.

The first PLL has a large bandwidth and is used to extract the clock from the incoming SDI signal and to de–serialize it. The clock is divided down to the parallel data–rate and this new clock is used to latch the data words into a FIFO buffer.

The data words are read out of the FIFO buffer using a second clock provided by a crystal–stabilized high–Q PLL with a narrow bandwidth. The resulting SDI output is nearly jitter–free.

Fig. A3 shows an example of a digital–to–analogue converter which is fed with the SDI output, and a clock signal provided by the high–Q PLL of the jitter remover.

If the system is fed with a studio reference signal, in genlock mode, any jitter on the reference signal must be removed before it is applied to the high–Q PLL; otherwise the jitter will be transferred onto the output signal.

A3. Jitter characteristics of the SDI receiver

Owing to the self–clocking characteristic of the NRZI code used in the SDI, the SDI receiver has to extract the clock from the incoming serial data–stream to permit data recovery. The timing relationship between the data and the clock signal must be maintained throughout the signal path. In other words, if the serial data–stream is clocked, the clock has to follow through the same changes in timing as the incoming data in order to guarantee distortion–free clocking.

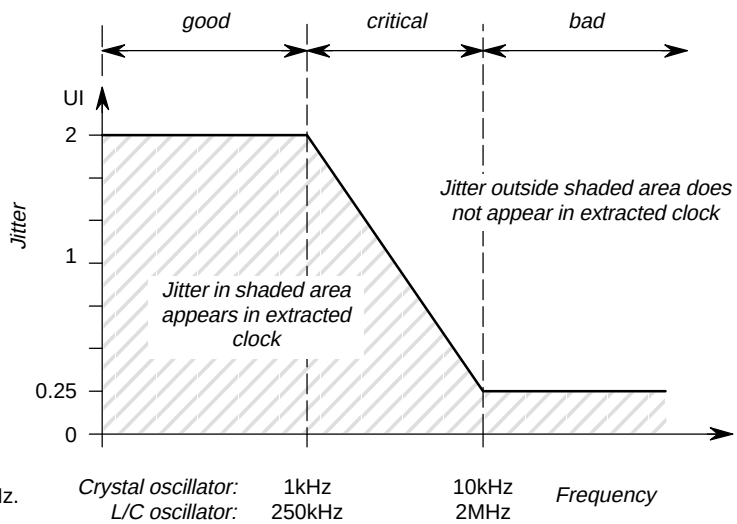
The accuracy with which the receiver PLL can lock on to the incoming signal and follow the incoming jitter depends on the PLL bandwidth – and it determines the performance of the SDI system. Consider a receiver PLL which has a bandwidth of 10 MHz; incoming jitter at frequencies up to 10 MHz will be transferred to the extracted clock. The timing between the data and the extracted clock will be maintained.

If jitter above 10 MHz occurs, it will not be transferred to the extracted clock. The timing between the data and the extracted clock will be distorted and latching errors can occur.

A standard receiver PLL consisting of an L/C loop filter can easily lock onto several clock frequencies, and, by virtue of its large capture range, it can in principle automatically adjust to various digital standards having data–rates between 270 and 140 Mbit/s.

It is clear that, since the PLL is capable of following the jitter up to the limits of its inherent bandwidth (and subject to the jitter transfer function of the PLL), any low–frequency jitter will be increased substantially before any error occurs on the re–clocking side. In the case where an L/C filtered PLL is used, the maximum jitter frequency, and the jitter amplitude, can become quite large.

High–precision equipment, such as a precision digital–to–analogue converter, has, in addition to the normal 270–Mbit/s PLL, a second, crystal–stabilized PLL operating at 27 MHz. This second PLL has a narrow jitter transfer function of a few kiloHertz only (see *Fig. A4*).



Note: 1 UI = 3.7ns at 270 MHz.

Fig. A4 – Jitter response of an SDI receiver.

When measurements are taken on receivers, the type of jitter (low, middle or high–frequency) should be identified and a record should be made of the type of PLL used.

Jitter in each of the three frequency ranges has strikingly different effects on the re–clocking device, depending on its amplitude [4][10]:

"Good" jitter

Jitter frequencies which lie within the clock recovery range of the PLL will be fully transferred to the recovered clock signal. Therefore, the timing relationships between the data and the extracted clock signal remain the same. Large jitter amplitudes can be tolerated.

"Critical" jitter

Jitter in the middle frequency range near to the edges of the PLL bandwidth (about 1 to 10 MHz for an L/C PLL, 1 to 10 kHz for a crystal–controlled PLL) will be partly transferred to the recovered clock signal. This means that the timing relationship between the data signal and the clock signal will be partly distorted. Jitter amplitudes which exceed about 0.25 UI can lead to errors (*Fig. A4*).

"Bad" jitter

Jitter frequencies falling outside the PLL bandwidth (greater than about 10 or 15 MHz for an L/C PLL, or greater than 100 kHz for a crystal–controlled PLL) will not be transferred to the regenerated clock. The timing relationship between the data signal and the extracted clock can therefore be distorted. Even small jitter amplitudes can cause re–clocking errors in this case.

A4. Effects of jitter in the SDI environment

Low–frequency jitter

Problems can arise with devices at the periphery of a digital studio such as digital–to–analogue converters and PAL encoders. Specific difficulties may occur in systems which have digital audio embedded within the SDI, or if the SDI is used to derive an audio reference.

High–frequency jitter

High–frequency jitter can cause bit–errors.

A4.1. Problems at the periphery of an SDI studio

Digital–to–analogue converters

Jitter will generate linearity errors in a D/A converter. The jitter tolerance should be less than 1 ns for the video signal and less than 0.1 ns for a 16–bit audio signal. This means that if the SDI signal is used to derive the clock for an audio D/A converter, special care must be taken to remove the jitter. A technique for jitter removal is discussed in *Section A2*.

PAL encoders

In a PAL encoder, jitter can cause a deviation of the subcarrier–to–line sync phase (ScH) or line jitter (H–jitter). A jitter amplitude of 0.7 ns in the SDI signal will cause a PAL phase jitter of 1°.

Interface to telecommunication networks

If the transport layer of telecommunications systems are used which have data–rates higher or lower than the data–rate of the SDI, problems may be caused by bit–stuffing and similar processes.

A4.2. Jitter in the SDI signal caused by a studio reference or a genlock signal

In most digital studios, the 270 Mbit/s signal is derived from the line–frequency (H signal) of an analogue reference signal. A "black burst" signal, used as such a reference and having a 4–ns jitter, can generate a jitter of 4 ns at the 270 Mbit/s level. This corresponds to more than one period (1 UI) of the 270 Mbit/s signal and lies outside the tolerance allowed in the SDI specification. A receiver using an L/C PLL re–clocking device can track this jitter easily, provided the jitter frequency is low.

Jitter of ± 3 ns is allowed in the parallel interface. If a parallel signal with just–acceptable jitter is converted to the serial data–rate by means of a serializer, the parallel jitter will also be transferred to the serial signal. It will also be outside the tolerances accepted for the SDI and may cause errors in subsequent equipment. Again, a receiver PLL can track this jitter if the frequency is sufficiently low.

Further discussion on this topic will be found in *Section 5.3.1.* and [2][6][7][10].

A5. Jitter measurement

A5.1. Clock extractor

Several of the jitter measurement methods described in *Chapter 4.* require the use of a "clock extractor". This is a device which is able to extract the clock from the incoming serial digital stream and deliver it in a variety of forms suitable as input to measurement instruments.

The clock extractor comprises three sections, each having a separate output. A block diagram is shown in *Fig. A5*.

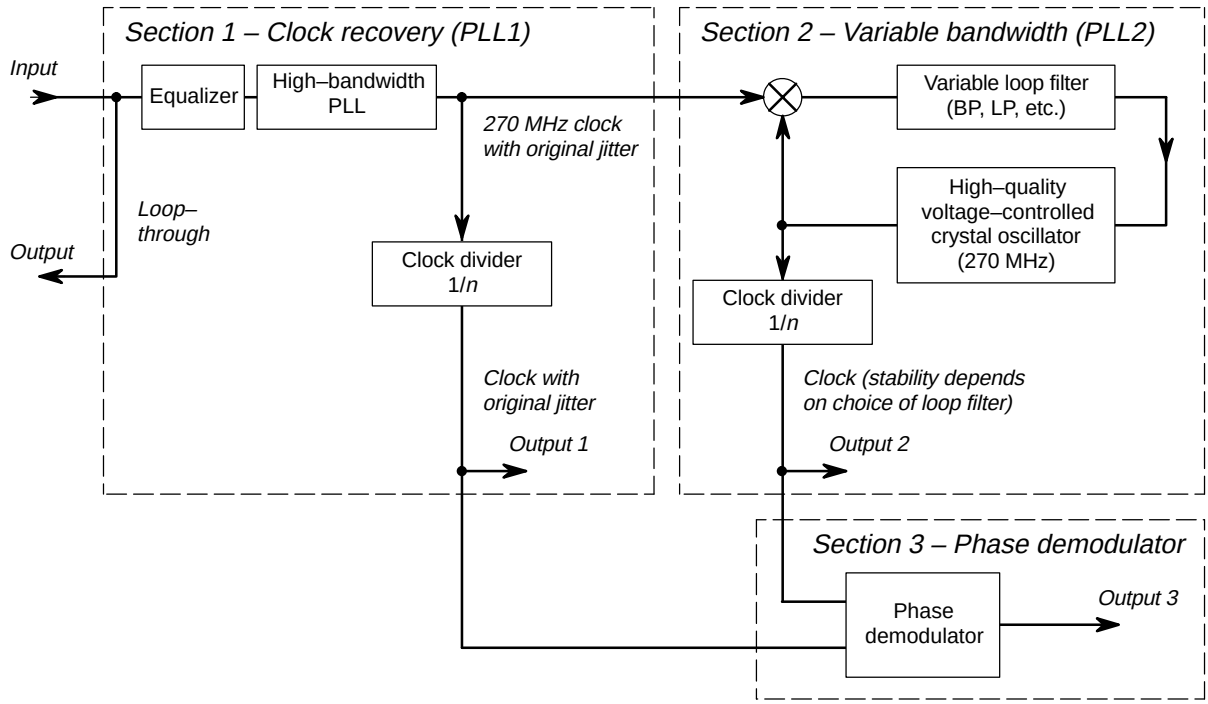


Fig. A5 – Block diagram of the clock extractor with phase demodulator.

Section 1 – output to spectrum analyzer

The front–end of this section has a loop–though of the serial digital signal, providing a connection to the unmodified incoming jitter.

The remaining circuits in this section consist basically of a wide–band clock recovery circuit which deliver to output 1 an SDI carrier clock signal with nearly the same jitter characteristics as the incoming SDI signal. This SDI carrier has no signal modulation and the sidebands only contain the jitter frequencies. Output 1 can be used to feed a spectrum analyzer.

When jitter in excess of 1 UI is to be measured, the serial clock divider is put into operation in order to obtain measurable jitter edges on the oscilloscope display. The value n is chosen according to the amount of jitter to be measured and the value can affect the measurements. The smallest possible value of n should be used. For example, if the jitter is close to 1 UI then $n = 3$ should be chosen. If the jitter is greater than 1 UI, then n should be increased. A value of $n = 10$ is normally acceptable, although it may mask word–correlated jitter components. The divider value n should be recorded alongside the jitter measurement results in the test record.

The output frequency is 270 MHz for normal operation, and 270/n MHz when measuring jitter of more than 1 UI, where n is the division ratio of the serial clock divider.

Section 2 – output to trigger an oscilloscope

This section comprises a phase–locked loop (PLL) with two selectable bandwidths. These permit the selection of two different jitter transfer functions.

The slopes of the bandpass characteristics should be 6 db/octave or greater, and the stop–band rejection should be at least 20 dB. The passband ripple should be less than ± 1 dB.

With a suitable choice of loop filter, the extracted clock will follow the jitter of the serial digital signal. It should be noted that the system measures jitter frequencies which are *outside the PLL bandwidth*. For example, if the clock recovery bandwidth is set to a cut–off frequency of 1 kHz, the extracted clock will follow jitter on the serial digital signal up to a frequency of 1 kHz.

Jitter at frequencies above 1 kHz can be measured if this extracted clock signal is used to trigger an oscilloscope and the incoming serial digital signal is observed.

The output frequency is 270 MHz for normal operation, and 270/*n* MHz when measuring jitter of more than 1 UI, where *n* is the division ratio of the serial clock divider.

Section 3 – phase demodulator output, to feed a spectrum analyzer or FFT oscilloscope

The phase demodulator measurement method is widely used in the telecommunications industry for jitter measurements and is very useful, especially in the frequency range up to 5 MHz. However, this does not cover frequencies up to 27 MHz, as specified for the verification of SDI performance.

The phase demodulator is fed with the outputs of sections 1 and 2 of the clock extractor.

The output of the phase demodulator is connected to a spectrum analyzer of an oscilloscope with the ability to display fast–Fourier transforms (FFT). The jitter spectrum with its specific jitter frequencies can then be observed [10].

Appendix B

Equalization and dynamic range in SDI receivers

This Appendix gives background information on several topics relating to the performance of data receivers used in SDI systems.

It is important to make a clear distinction between automatic equalizer operation and the dynamic range of the input amplifier of an SDI receiver. Equalizer operation is dependent essentially on signal amplitude and cable length, while the dynamic range relates to low–frequency limitations.

B1. Cable equalization

It is recommended that in any studio installation, a safety margin of 6 dB, corresponding to about 80 m of cable length, should be reserved, in relation to the maximum equalization capability of the SDI receivers used. During installation, and in subsequent testing, "stress" tests should be performed by inserting additional lengths of cable and verifying that performance is not degraded.

If it is found that the maximum length of cable that can be tolerated by the system is different to a significant degree, according to the type of test signal used (for example, 5 or 10 m difference between a colour–bar signal and the SDI check field), then this might indicate a design problem.

In theory the receiver equalization characteristic should be exactly the inverse of the cable characteristic, but practical equalizers may have slightly different responses. If this is the case, then the tracking of the $1 / \sqrt{f}$ response of the cable and the inverse response of the equalizer will not match. To highlight any failings of the equalizer, tests should therefore be carried out with a range of cable lengths between the minimum and maximum for which the equalizer is designed.

Fig. B1 shows graphs of error performance as a function of SDI signal level and cable length, for two test signals. With the colour–bar signal the system performs consistently well, but for the SDI check field test signal, the system malfunctions over a range of cable lengths from about 80 to 140 m if the SDI signal level is 850 mV. It should be noted that this level is *within* the specified tolerance of 800 mV ± 10%. This problem has been encountered in equipment using certain receiver chip–sets.

B2. Dynamic range

The SDI check field has long sequences of logic "0"s which occur repeatedly along a full horizontal line. These sequences produce two types of low–frequency effect:

– The first is similar to a change of average picture level (APL) in analogue video systems and can necessitate a much larger dynamic range in amplifiers after certain forms of coupling circuit. If the coupling is capacitative, the use of a larger capacitor will usually improve performance, but there is no easy solution if inductive coupling is used.

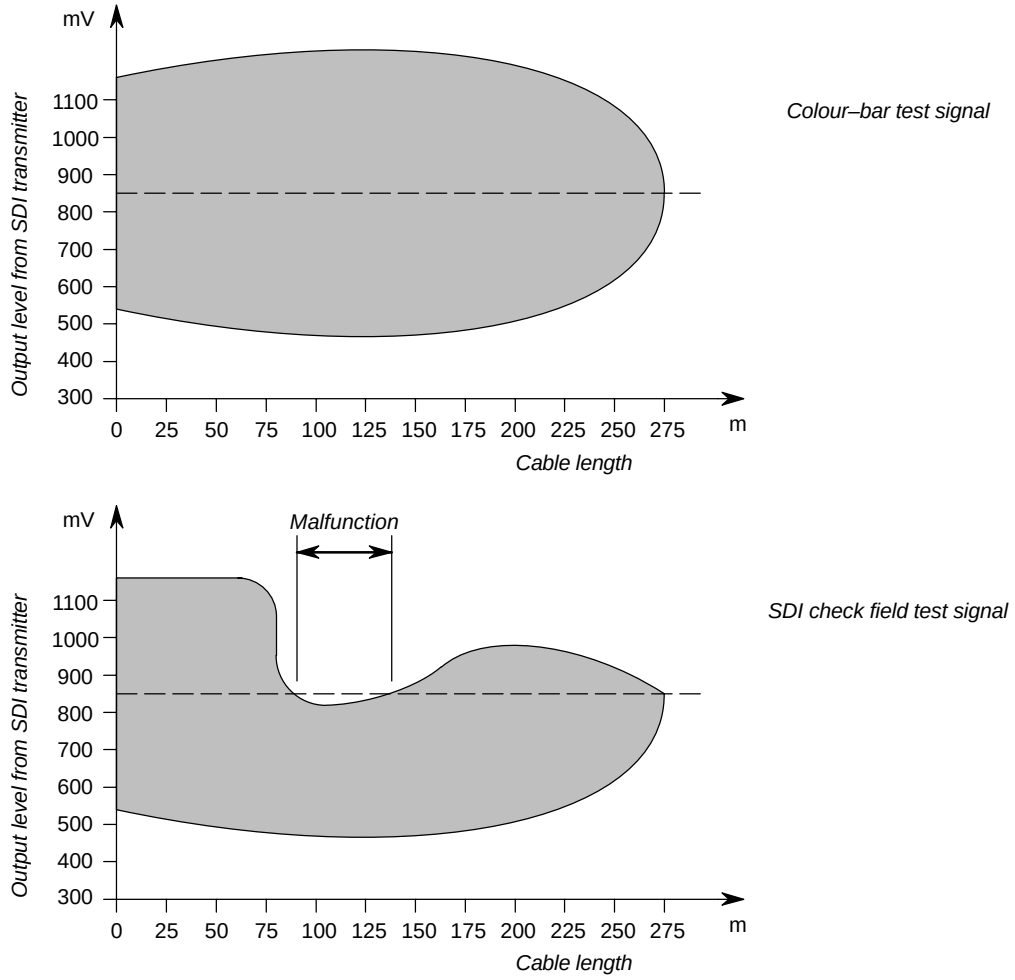


Fig. B1 – Examples of cable equalization range, showing dependence on test signal content.

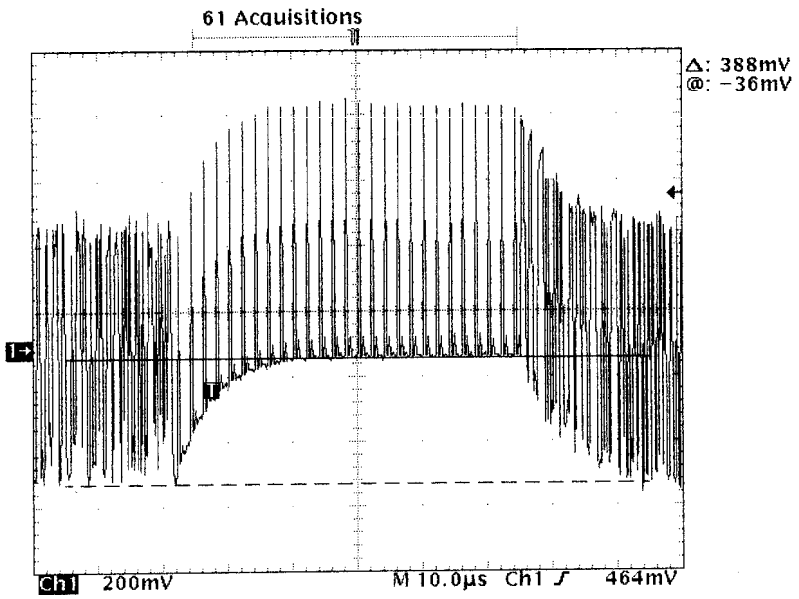


Fig. B2 – Example of DC shift in an SDI signal.

If a system fails to operate correctly when carrying the SDI check field, it may not be caused by an equalizer problem. Instead, it might be a combination of insufficient dynamic range of the amplifier and waveform distortion caused by the coupling.

– The other part of the SDI check field produces low–frequency energy only, without a DC level shift; this tests the equalizer as well as the phase–locked loop (PLL).

The DC shift of the test generator and the design of the output amplifier of the SDI transmitter can add to this effect (see *Fig. B2*).

Appendix C

Market survey of measurement equipment for digital video signals
(June 1995)

Many of the measurement methods described in this document require the use of sophisticated test and measuring instruments. To assist readers in the selection of equipment meeting their specific needs, the EBU conducted a survey of test instruments known to be available on the European market in June 1995. This Appendix gives a brief description of the equipment, based essentially on the manufacturers' own promotional materials and/or equipment handbooks. The tables in *Section C9.* give a comparative summary of the measurement options of the instruments presented here.

The mention of specific manufacturers, or specific products, does not imply that other sources of suitable equipment do not exist, and does not imply any preference on the part of the European Broadcasting Union in favour of any particular products and manufacturers.

The EBU is grateful to the manufacturers for their contributions to this survey.

C1. AAVS model DSA 309

Manufactrurer: AAVS
222–226 rue de Rosny
F–93100 Montreuil
France

The DSA 309 is an all–format digital video analyser for the testing of component and composite digital video signals in both 525 and 625–line formats.

Continuous real–time on–line measurement of all key parameters permits "live" monitoring of the following peformance characteristics:

– serial jitter;
– colour levels;
– EDH errors;
– bit activity;
– signal amplitude;
– parity bit errors;
– timing reference signal (TRS) errors;
– reserved code word errors;
– non–recommended code value errors.

Real–time colour level monitoring permits the detection of "illegal" colours.

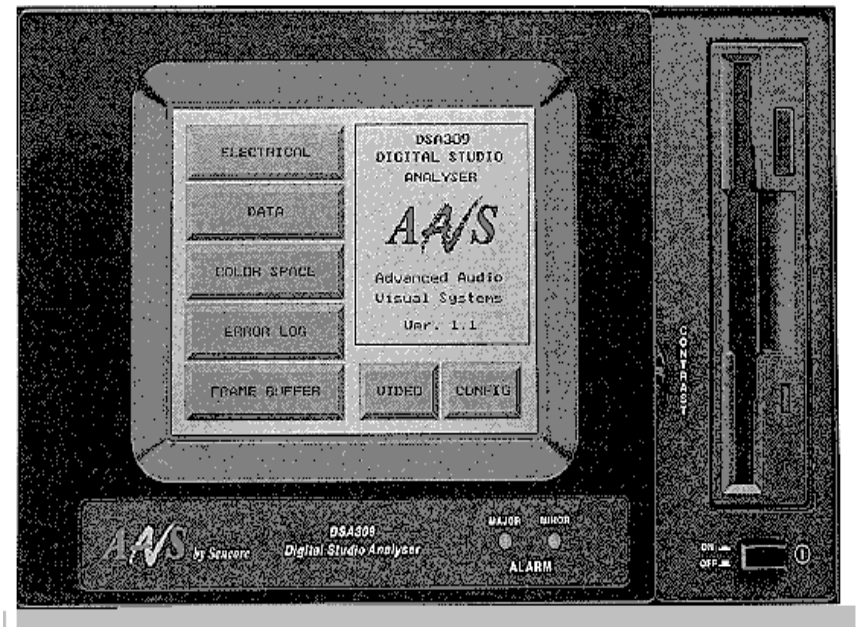


Fig. 16 – AAVS model DSA 309 measurement set

Error logging permits system performance monitoring and documentation or storage on the built–in LCD display, an external printer or the built–in 3 1/2–inch floppy disk drive.

The alarm in the user interface provides notification when user–defined thresholds are exceeded.

Comprehensive digital displays, complemented by simulated analogue waveform equivalents, help to bridge the gap between analogue and digital testing environments, thereby creating a user–friendly interface for both operators and engineers.

Operation and handling of the equipment is by means of a touch–screen display.

C2. AAVS model S310

Manufactrurer: AAVS
222–226 rue de Rosny
F–93100 Montreuil
France

The S310 is a modular test measurement set for serial and parallel video signals. Four modules are available:

Maintenance module (S310–3)

This is a service module for conducting maintanence on digital video eqauipmnt. It has five BNC outputs for the following signals:

– field pulses (F);

– vertical pulses (V);

– horizontal pulses (H);

– service sync;

– output

The signal delivered at the “output” connector is selected using the keypad, depending on the type of test to be carried out.

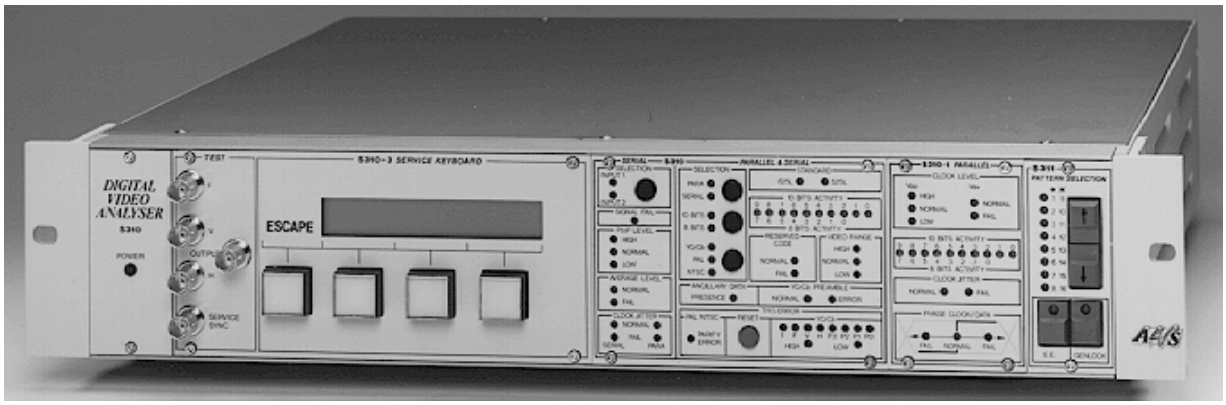


Fig. 17 – AAVS model S 310 with integrated pattern generator S 311

Parallel and serial module (S310)

This is a supervisory module for parallel and serial signal characteristics. It can be set by the user to monitor parallel or serial bit–streams in 8 or 10–bit mode, carrying Y,C_R,C_B, PAL or NTSC. Front–panel LEDs give the following indications:

peak–to–peak signal amplitude	high, normal, low
average level	normal, fail
clock jitter	normal, fail
standard	625 / 525
bit activity	0 ... 9
preamble	normal, fail
reserved code	normal, fail
ancillary data	presence
TRS error	high, low, 0 ... 7 (with reset button)
video range	high, normal, low
parity error	

Parallel module (S310–1)

This module provides additional indications for the following characteristics of a parallel interface signal:

amplitude (peak–to–peak)	high, normal, low
amplitude (mean)	normal, fail
bit level	0 ... 9
clock jitter	normal, fail
clock/data phase	fail – normal – fail

Pattern generator (S311)

This module provides a choice of 15 built–in test patterns, and the possibility of downloading a 16th pattern created on a personal computer. The pattern module can be genlocked to an analogue black burst signal, or to a digital video signal.

C3. Pixel Power model PC601 Framestore

Manufacturer: Pixel Power Ltd.
Nuffield Road
Cambridge, CB4 1TG
United Kingdom

The PC601 is a PC–based digital framestore with software for waveform and vector displays, hex–dump and data checks. The functions and displays of this system are illustrated in *Fig. 18*.

Main menu

```
PC601 Framestore Engineering Routines  Ver 2.2  (c) Pixel Power Ltd. 1992,1994

 Engineering Menu

  K Toggle Lock Source (analogue)

  P Preview Is Off
  G Grab Frame

  B Displaying Data As 10 Bits
  L Set Line Number (1)

  C Check Data
  D Discrepancy check
  T Test Pattern

  M Examine Memory
  E Examine Line
  W Waveform Display
  V Vectorscope Display

  Q Quit From Engineering Routines

 Status
```

Hexdump of a selected line

PC601 Framestore : Displaying Line 100 (page 6)

SMPL	VALUE	SMPL	VALUE	SMPL	VALUE	SMPL	VALUE
Cb 0436	80.0	Y1 0437	EB.0	Cr 0438	80.0	Y2 0439	EB.0
Cb 0440	80.0	Y1 0441	EB.0	Cr 0442	80.0	Y2 0443	EB.0
Cb 0444	80.0	Y1 0445	EB.0	Cr 0446	80.0	Y2 0447	EB.0
Cb 0448	80.0	Y1 0449	EB.0	Cr 0450	80.0	Y2 0451	EB.0
Cb 0452	80.0	Y1 0453	EB.0	Cr 0454	80.0	Y2 0455	EB.0
Cb 0456	80.0	Y1 0457	EB.0	Cr 0458	80.0	Y2 0459	EB.0
Cb 0460	80.0	Y1 0461	EB.0	Cr 0462	80.0	Y2 0463	EB.0
Cb 0464	80.0	Y1 0465	EB.0	Cr 0466	80.0	Y2 0467	EB.0
Cb 0468	80.0	Y1 0469	EB.0	Cr 0470	80.0	Y2 0471	EB.0
Cb 0472	80.0	Y1 0473	EB.0	Cr 0474	80.0	Y2 0475	EB.0
Cb 0476	80.0	Y1 0477	EB.0	Cr 0478	80.0	Y2 0479	EB.0
Cb 0480	80.0	Y1 0481	EB.0	Cr 0482	80.0	Y2 0483	EB.0
Cb 0484	74.0	Y1 0485	EB.0	Cr 0486	82.0	Y2 0487	E8.0
Cb 0488	48.0	Y1 0489	DF.0	Cr 0490	89.0	Y2 0491	D5.0
Cb 0492	1C.0	Y1 0493	D2.0	Cr 0494	90.0	Y2 0495	D2.0
Cb 0496	10.0	Y1 0497	D2.0	Cr 0498	92.0	Y2 0499	D2.0
Cb 0500	10.0	Y1 0501	D2.0	Cr 0502	92.0	Y2 0503	D2.0
Cb 0504	10.0	Y1 0505	D2.0	Cr 0506	92.0	Y2 0507	D2.0
Cb 0508	10.0	Y1 0509	D2.0	Cr 0510	92.0	Y2 0511	D2.0
Cb 0512	10.0	Y1 0513	D2.0	Cr 0514	92.0	Y2 0515	D2.0
Cb 0516	10.0	Y1 0517	D2.0	Cr 0518	92.0	Y2 0519	D2.0
Cb 0520	10.0	Y1 0521	D2.0	Cr 0522	92.0	Y2 0523	D2.0

↑ previous line ↓ next line PgUp previous page PgDn next page Esc exit

Fig. 18 – Pixel Power PC 601 software displays

Waveform display

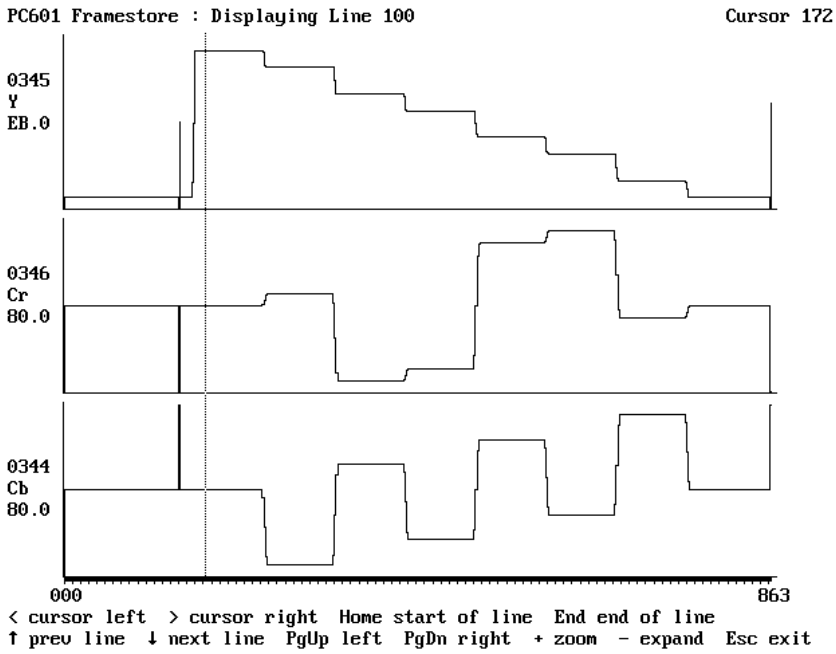


Fig. 18 (contd) – Pixel Power PC 601 software displays

C4. Rohde & Schwarz model VCA

Manufacturer: Rohde & Schwarz
Postfach 80 14 69
D–81671 München
Germany

The model VCA digital component video analyseris designed for both parallel and serial signals. It provides a quasi–analogue display and a tabluar display of the data in the video signal using its built–in LCD display. Features include the possibility of measuring jitter, spectrum analysis, return loss and delay (using an external genlock facility).

The functions of the VCA analyser fall into two groups:

Oscilloscope functions:

– overlaid waveform display of several lines from different fields;

– waveform with line selector;

– hex–dump display of all video data.

Measurement functions:

– TRS errors;

– reserved code errors;

– video range errors;

– CRC errors;

– gain–delay errors;

– jitter spectrum;

– jitter time;

– amplitude spectrum;

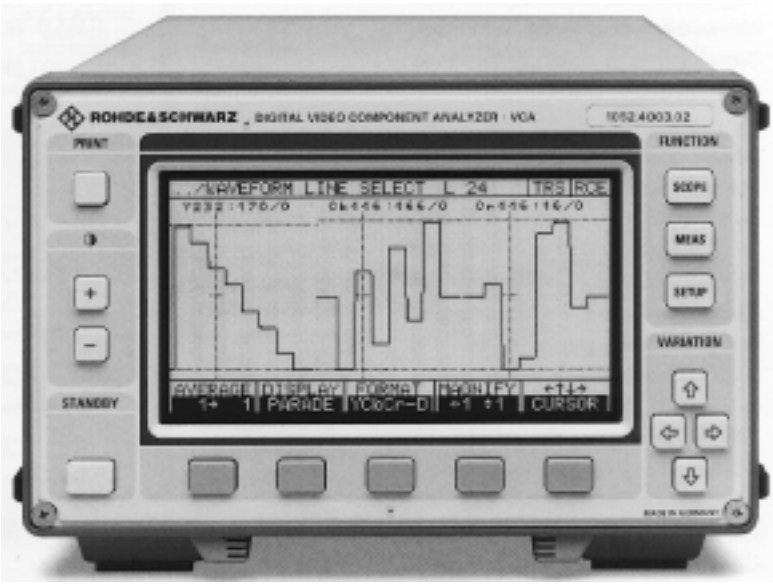


Fig. 19 – Rohde & Schwarz model VCA video analyser

– return loss;

– signal delay.

The unit offers several other features, including:

– format errors can be shown as an error rate or a history display;

– averaging;

– theoretical waveform filtering in accordance with ITU–R Recommendation BT.601;

– remote control via RS 422 interface (configurable for RS 232 operartion);

– print–screen options to an external line printer via RS 232 interface.

C5. Tektronix model SDA 601

Manufacturer: Tektronik Inc, USA
PO Box 500M/S 50–439
Beaverton, OR 97077
USA

The Tektronix SDA 601 serial digital analyser gives a quick overview of the digital video signal. It detects and identifies data format and video format errors, indicates the EDH status (SMPTE Recommended Practice RP165), and reports on any other ancillary data.

The information is displayed on the built–in display or on an external picture monitor; its can also be transferred directly to a computer or a printer via an RS 232 interface.

The SDA 601 analyser can verify that the Y, C_B, C_R signal components are within their system limits. It can also store reference signals and store a video frame after the detection of an error.

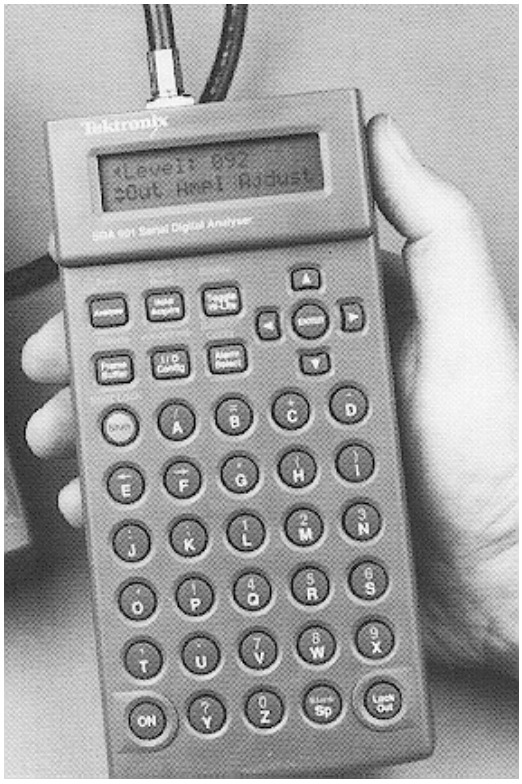


Fig. 20 – Tektronix SDA 601 serial digital video analyser

C6. Tektronix models WFM 601 and WFM 601i

Manufacturer: Tektronik Inc, USA
PO Box 500M/S 50–439
Beaverton, OR 97077
USA

The Tektronix 601i is a self–contained component waveform/vector monitor. It displays the serial digital colour–difference signals, after internal D/A conversion, in one of several forms: vector, lightning, diamond, bow–tie mode, or in a parade/waveform mode in RGB or Y, C_B, C_R format.

In the physical domain, the 601i version also displays the (sampled) eye–pattern of the serial digital video signal.

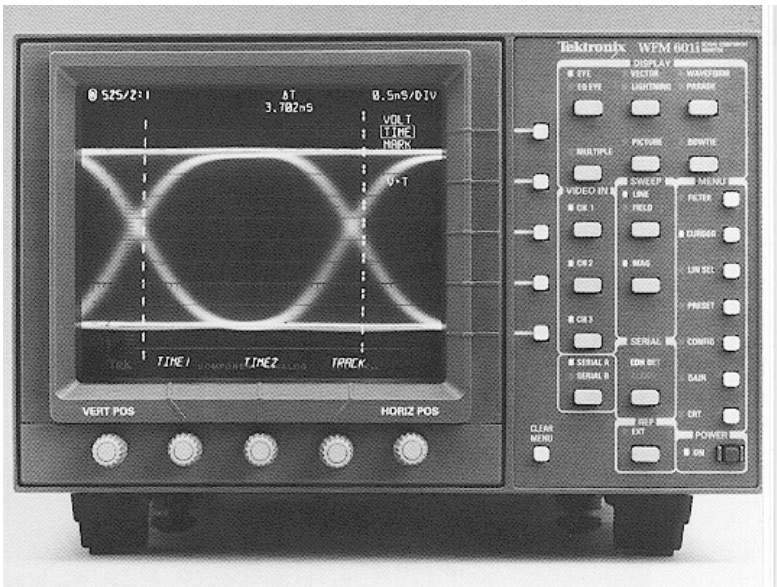


Fig. 21 – Tektronix WFM 601i serial digital waveform monitor

Other features are:

– timing and level cursors;

– line selector;

– picture monitor;

– ancillary data and EDH detection and handling system;

– RGB or Y, C_B, C_R analogue monitor output with selectable gamut indication;

– front–panel indication (LED) for transmission or format errors;

– posibility for genlocking to an external analogue black–burst reference.

C7. Viewtronix linestore with Digiview software

Manufacturer: Viewtronix Ltd.
Butts Road
Woking
GB–Surrey GU21 1JU
United Kingdom

The Digiview system consists of a PC–based digital linestore and software for examination of the digital data line. It has a parallel input, with a serial input available as an option.

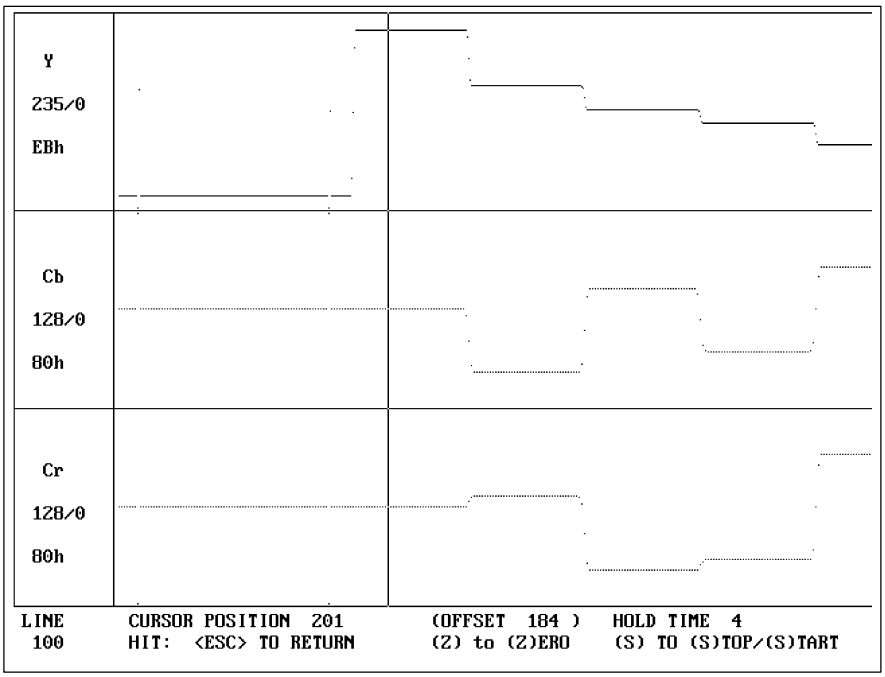


Fig. 22 – Waveform display of Digiview software

The system displays the data at the cursor position, in hexadecimal (8–bit or 10–bit values) and in decimal. Each sample can be displayed individually. It features a non–real–time TRS check facility, can be triggered externally and provides an output to an analogue monitor with a cursor highlighting the current position.

The menu options include the following functions:

– system configuration:	8 or 10 bits, trigger mode (random, line error, external), cycle mode
– trigger data capture	
– view and measure current data:	tabular data display: waveform display (de–multiplexed components) full–line component display single component waveform display overview (all data, not de–multiplexed) direct display (not de–multiplxed) vector display bit activity
– compare data	comparison with data stored on hard–disk
– file control	save/load data to/from hard–disk
– auto–check TRS	non real–time timing reference signal verification
– ancillary data	display all data after ANC preamble
– look for sequence	triggers when a pre–determined data sequence occurs
– production test with stored data	TRS check and comparison of several lines

C8. Viewtronix linestore with RBT software

Manufacturers: linestore: Viewtronix Ltd.
Butts Road
Woking
GB–Surrey GU21 1JU
United Kingdom

software: Rundfunk Betriebstechnik GmbH (RBT)
Videotechnik
Wallenstein stasse 119
D–90431 Nürnberg
Germany

The Viewtronik/RBT system consists of a PC–based digital linestore and software for examination of the digital data line. It has a parallel input, with a serial input available as an option.

It features a display of hexadecimal and decimal data values at the cursor position and the corresponding analogue levels (mV). 8 and 10–bit display is provided, and notation in accordance with [S.5]. It displays individual samples, or uses a linear spline. It has a timing cursor and uses the sampling structure defined in [S.3]. Timing reference signals can be checked in non real time. An analogue signal is provided for the connection of a moinitor; this includes a line cursor.

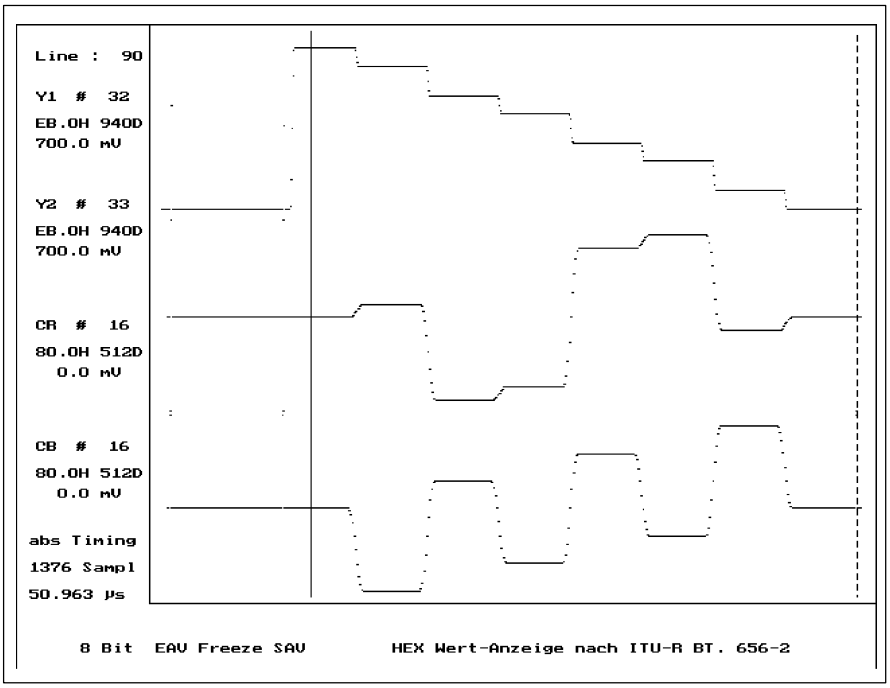


Fig. 23 – Waveform display of RBT software

C9. Summary of test equipment features

Table 8 – Measurements in the physical domain

	DSA 309	S 310	PC 601	VCA	SDA 601	WFM601i	Digiview	RBT
Eye pattern						yes		
Signal level	yes	yes		note 1	yes	yes		
Signal ripple	yes	yes						
LF signal level distortion	yes	yes						
DC offset	yes	yes				yes		
Overshoot						yes		
Rise and fall times						yes		
Return loss				note 2				
All–frequency jitter	yes	yes		yes		yes		
Weighted jitter (simplified)	yes			note 3		yes		
Weighted jitter (jitter spectrum)				note 3				
Cable length simulation				note 4				

Notes: 1 with “amplitude spectrum” option
2 with “return loss” option and external bridge
3 with “jitter spectrum” option
4 included in software up–grade, July 1995

Table 9 – Measurements in the data domain

	DSA 309	S 310	PC 601	VCA	SDA 601	WFM601i	Digiview	RBT
Active bits (8/10)	yes	yes	yes	yes	yes	yes	yes	yes
ITU–R 656–1 notation			yes					yes
Digital signal levels in:								
binary	yes			yes				
hexadecimal	yes	note 1	yes	yes	yes		yes	yes
decimal	yes	note 1		yes			yes	yes
mV				yes		note 2		yes
Check for reserved words	yes	yes	yes	yes	yes	yes	yes	yes
TRS check	yes	yes	yes	yes	yes	yes	yes	yes
Rise and fall times						note 3		
CRC check				yes	yes	yes		
Compare current and transmitted CRC codes (EDH)	yes				yes	yes		
Luminance/chro-minance delay				yes		note 4		
Picture position w.r.t. TRS				yes				

	DSA 309	S 310	PC 601	VCA	SDA 601	WFM601i	Digiview	RBT
Ancillary data	yes	yes	yes	yes	yes	yes	yes	yes
Type/Length identification	yes				yes	yes		
Video range	yes	yes	yes	yes	yes	yes		
Colour gamut check	yes		yes			yes		
Delay in SDI equipment				note 5		yes		

Notes: 1 hexadecimal or decimal, depending on software version

2 by means of level cursors

3 by means of timing cursors; dependent on internal D/A conversion and filtering

4 with bow–tie signal

5 with “signal delay” option

Table 10 – Measurements in the physical domain

	DSA 309	S 310	PC 601	VCA	SDA 601	WFM601i	Digiview	RBT
Analogue monitoring	yes					yes	note 1	note 1
External alarm (e.g. EDH fault)	yes				yes	yes		

Notes: 1 luminance (Y) only

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