EBU INTERFACES FOR 625–LINE DIGITAL VIDEO SIGNALS AT THE 4:4:4 LEVEL OF CCIR RECOMMENDATION 601

Tech. 3268–E – Second edition January 1992

CONTENTS

2nd edition – Note

The interfaces specified in this second edition of EBU document Tech. 3268 are identical to those specified in the first edition, issued in June 1991.

Errors in the first edition have been corrected, and the presentation of *Figs. 2* and *4* has been clarified.

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Introduction

This document describes the means of interconnecting digital television equipment operating in the 625–line standard and complying with the 4:4:4 encoding parameters defined in CCIR Recommendation 601.

The interfaces for the 4:4:4 level are based on the use of parallel and serial interfaces already developed for use at the 4:2:2 level. These are described in EBU document Tech. 3267 “EBU interfaces for 625–line digital video signals at the 4:2:2 level of CCIR Recommendation 601”. Whereas, at the 4:2:2 level, a single interface carries a multiplex of a wide–band luminance signal and two lower–bandwidth colour–difference signals, at the 4:4:4 level a pair of interfaces is used, each carrying a multiplex of two wide–band video signals. This gives capacity for conveying red, green, blue (R,G,B) primary signals or, alternatively, the luminance and two colour–difference signals together with a fourth wideband signal such as an associated key signal.

The interfaces for the 4:4:4 level have been specified for 10–bit data words. Thus they will carry not only 8–bit signals encoded according to CCIR Recommendation 601 but also 10–bit signals in which additional bits may have been generated during processing.

Only two devices will be connected together at one time through one interface.

This specification relates to both bit–parallel and bit–serial interconnections.

It may be noted that the electrical and mechanical characteristics of the 4:4:4 interfaces are identical to those of the 4:2:2 interfaces specified in EBU document Tech. 3267.

A list of definitions of terms used in this specification is given in *Appendix 1*, and relevant reference documents are listed in the *Bibliography*.

Nomenclature

In this specification, the contents of digital words are expressed in both decimal and hexadecimal forms, denoted by the suffixes “d” and “h” respectively.

To avoid confusion between 8–bit and 10–bit representations, the eight most–significant bits are considered to be an integer part while the two additional bits, if present, are considered to be fractional parts.

For example, the bit pattern 10010001 would be expressed as 145_d or 91_h, whereas the pattern 1001000101 would be expressed as 145.25_d or 91.4_h.

Where no fractional part is shown, it should be assumed to have the binary value 00.

Table 1 – Encoding parameter values for video signals at the 4:4:4 level.

Parameters	Specifications
Coded s	R, G, B *or* Y, C_R, C_B
Number of samples per total line – each R, G, B ignals *or* – luminance and each colour–difference signal	 864
Sampling structure	Orthogonal line, field and picture–repetitive.
Sampling frequency (nominal)	13.5 MHz
Form of coding	Uniformly–quantized PCM, 8 (optionally 10) bits per sample.
Number of samples per digital active line	720
Correspondence between video signal levels and quantization levels – R, G, B *or* luminance signal – each colour–difference signal	 220 quantization levels with black level corresponding to level 16 and peak–white level corresponding to level 235 225 quantization levels in the centre part of the quantization scale, with zero signal corresponding to level 128
Use of code words	Only levels 1 to 254 are available for coding the video signal

Chapter 1

Structure of signals transferred through the interfaces

1. General description

The interface consists of two uni–directional interconnections between one device and another. The interconnections carry the data corresponding to the television signal and associated data.

The two interconnections are referred to as “Link A” and “Link B”.

The data signals are carried as binary information in 10–bit words. These signals are:

– the video signals themselves;

– digital blanking data signals;

– timing reference signals;

– ancillary data signals.

These signals are time–multiplexed.

In the *parallel* interface, the 10–bit video data for each link is transferred across the interfaces on ten parallel data pairs together with a clock signal on an eleventh pair.

In the *serial* interface, the 10–bit video data for each link is transferred across the interface as a serial data–stream in unbalanced form and at an impedance of 75 ohms.

2. Video data signals

2.1. Coding characteristics

The video data signals are derived by coding of the analogue video signal components in accordance with the 4:4:4 level of CCIR Recommendation 601. These components are the gamma–corrected primary signals, or luminance and colour–difference signals derived from them. The main details of the coding parameters are reproduced in *Table 1*.

2.2. Video data word format

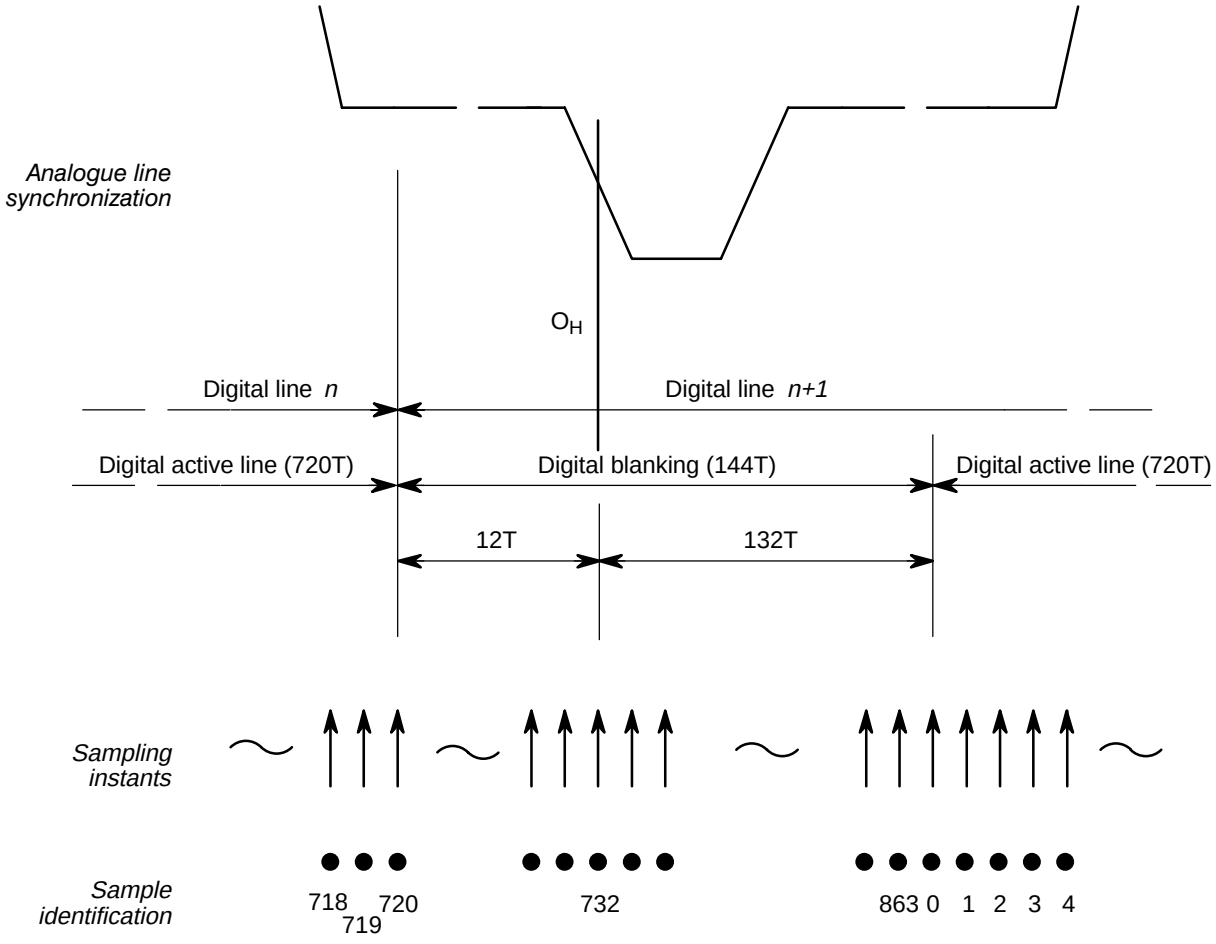
8–bit data words resulting from sampling according to CCIR Recommendation 601 are carried in the most–significant bits of the 10–bit interface signal. In this case the remaining LSBs should be set to logic “0”.

Words in which the eight most–significant bits are all set to “1” or are all set to “0” (i.e. 1111 1111 xx or 0000 0000 xx, where “x” represents bits which are either absent – the 8–bit case – or can have any value) are reserved for identification purposes. The corresponding data values are excluded from the data coding range.

2.3. Timing relationship between video samples and the analogue synchronizing waveform

2.3.1. Line

Fig. 1 shows the timing relationship between video samples and the analogue line synchronization.



Notes:

1. Digital blanking contains 144 samples, numbered 720 to 863 in the figure. The digital active line contains 720 samples, numbered 0 to 719 in the figure.
2. The position of digital blanking shown in the figure was chosen so that the digital active line is symmetrically disposed in relation to the permitted variations, specified relative to the line synchronization reference O_H, in the start and finish times of the analogue active line.
3. For identification purposes, word “0” is taken as being the first word of the digital active line.
4. O_H is the analogue line timing reference, set at the mid–amplitude point of the leading edge of the line synchronizing pulse.
5. T is the sampling period (10^3/13.5 ns)

Fig. 1 – Correspondence between the video samples and the analogue line synchronization.

2.3.2. Field

The start of the first digital field is fixed by the position specified for the start of the digital line. The first digital field starts 12 sample–periods before the start of analogue line no. 1. The second digital field starts 12 sample–periods before the start of analogue line no. 313.

Fig. 2 shows this relationship between the digital and analogue lines in the first and second fields of the television picture.

2.4. Multiplex structure

The video data words are conveyed in two separate 27–Mword/s data–streams.

2.4.1. R, G, B, (K) multiplex

The multiplex structure in links carrying colour primaries is as follows:

Link A $B_0\ G_0\ R_0\ G_1\ B_2\ G_2\ R_2\ G_3\ B_4$ .....
Link B $B_1\ K_0\ R_1\ K_1\ B_3\ K_2\ R_3\ K_3\ B_5$ .....

where R, G and B represent the red, green and blue signal data words and K represents the key signal data words (if present). The first sample of the digital active line shall be B_0 for link A and B_1 for link B. The distribution of the red, green, blue and key signals between link A and link B is shown in *Fig. 3a.*

2.4.2. Y, CR, CB (K) multiplex

The multiplex structure on links carrying luminance and colour–difference signals is as follows:

Link A $CB_0\ Y_0\ CR_0\ Y_1\ CB_2\ Y_2\ CR_2$ .....
Link B $CB_1\ K_0\ CR_1\ K_1\ CB_3\ K_2\ CR_3$ .....

where Y, CB and CR represent the luminance and colour–difference signals respectively, and K represents the key signal data words (if present). The first sample of the digital active line shall be CB_0 for link A and CB_1 for link B. The distribution of the luminance, colour–difference and key signals between links A and B is shown in *Fig. 3b*.

3. Digital blanking data

During digital blanking, the luminance or R, G, B sample values are set to black level (16.00_d – 10.0_h) and the colour–difference samples are set to zero level (128.00_d – 80.0_h), unless carrying ancillary signals. The key samples should be set to peak white level (235.0_d – $EB.0_h$) when not carrying a key signal or ancillary signal.

4. Video timing reference signals

4.1. General

Two video timing reference signals are multiplexed into the data–stream on every line, immediately preceding and following the digital active line data. These are denoted SAV (Start of Active Video) and EAV (End of Active Video). Their position in the data multiplex is shown in *Fig. 4*; they retain the same format throughout the field–blanking interval.

4.2. Timing reference signal format

Each timing reference signal consists of a four–word sequence.

The first three words are a fixed preamble. The fourth word contains information defining:

– first and second field identification;

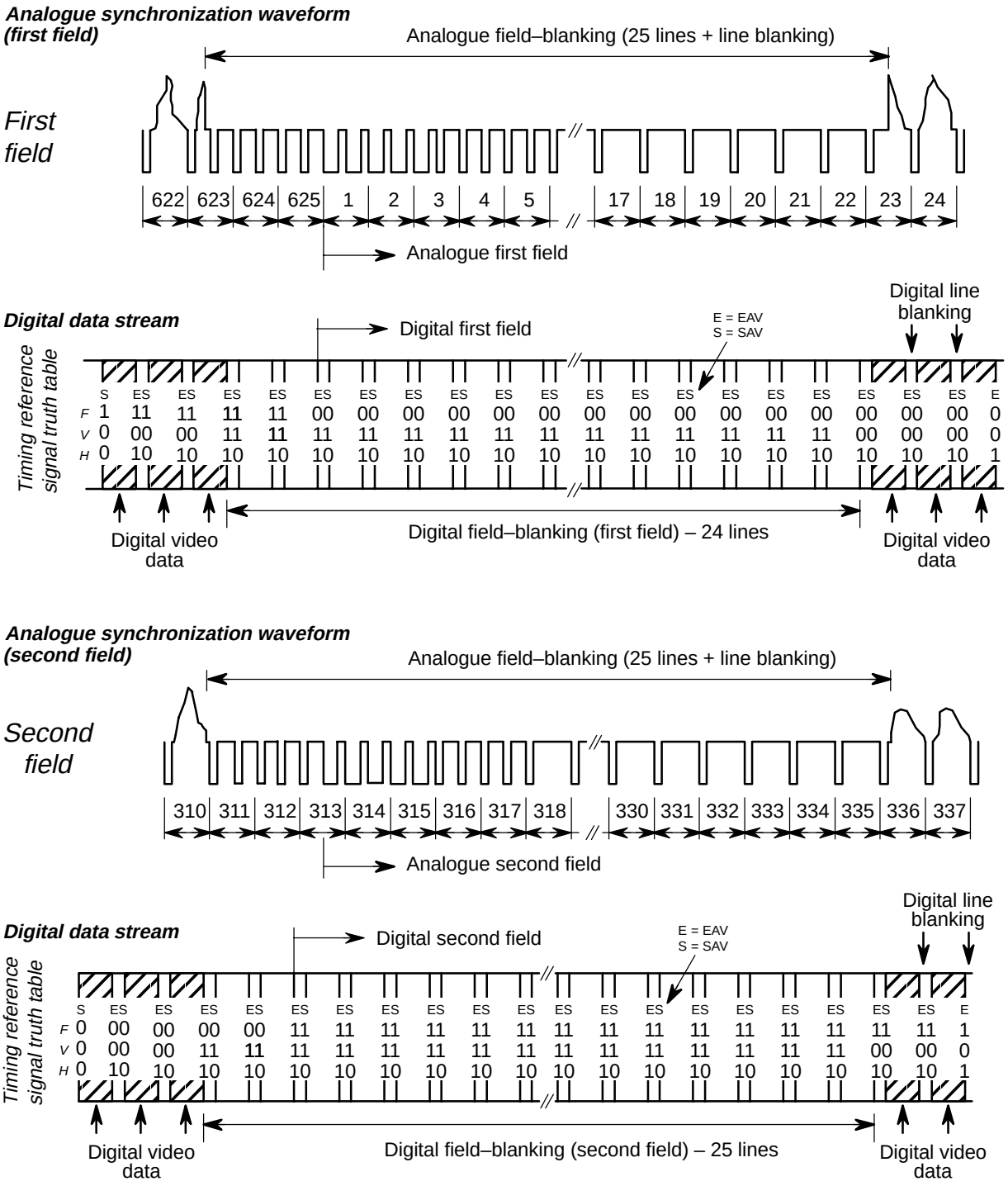
– state of the field–blanking;

– beginning and end of the line–blanking.

The sequence of four words can be represented, using 10–bit hexadecimal notation, in the following manner:

FF.C 00.0 00.0 XY.0

in which XY.0 represents a variable word.



Notes:

1. The allocation of active lines in the digital fields was arranged in such a way as to avoid the digital processing of half–lines. The number of active video lines is 288 in both fields, and the width of digital field–blanking is 24 lines preceding the active part of the first field and 25 lines preceding that of the second.

2 Blanking appropriate to the national broadcasting standard should be applied at the point at which the signal is converted to the analogue form.

Fig. 2 – Relationship between the digital and analogue fields, showing also the position of the digital field–blanking interval.

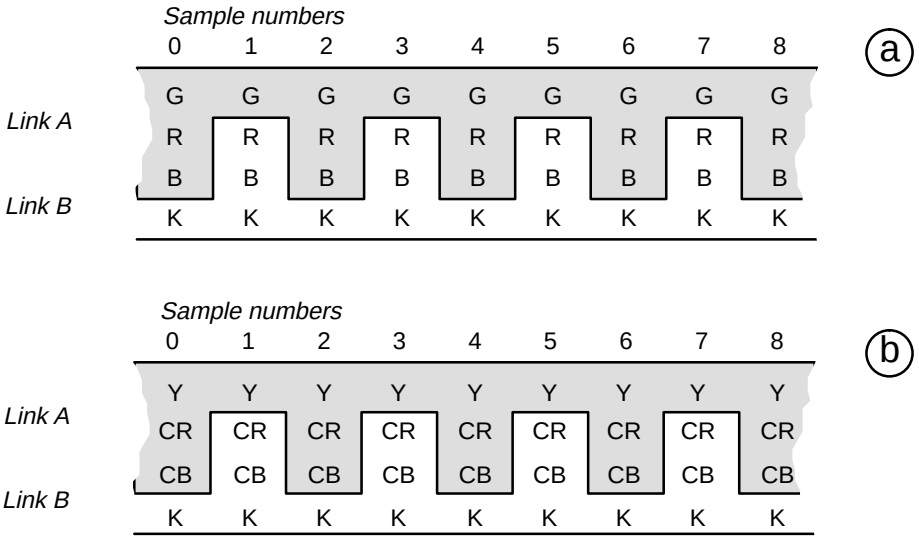


Fig. 3 – Link contents when carrying R, G, B, K and Y, CR, CB, K signals.

In binary notation, this same sequence corresponds to the values shown in *Table 2*.

The binary values of F, V and H characterise the three types of information listed at the beginning of this section:

F = “0” during the first field;

V = “1” during the field–blanking interval;

H = “1” at the start of the line–blanking interval.

Fig. 2 shows the states of the F, V and H bits in the digital timing reference signals, in the region about the field–blanking interval.

Bits P_3 to P_0 provide a limited error–detection and error–correction function on the F, V and H bits, as explained in *Appendix 2*. The binary values of P_3, P_2, P_1 and P_0 depend on the states of F, V and H, in accordance with *Table 3*.

Table 2 – Timing reference signal.

Data bit number	First word (FF.C)	Second word (00.0)	Third word (00.0)	Fourth word (XY.0)
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P_3
4	1	0	0	P_2
3	1	0	0	P_1
2	1	0	0	P_0
1	1	0	0	0
0	1	0	0	0

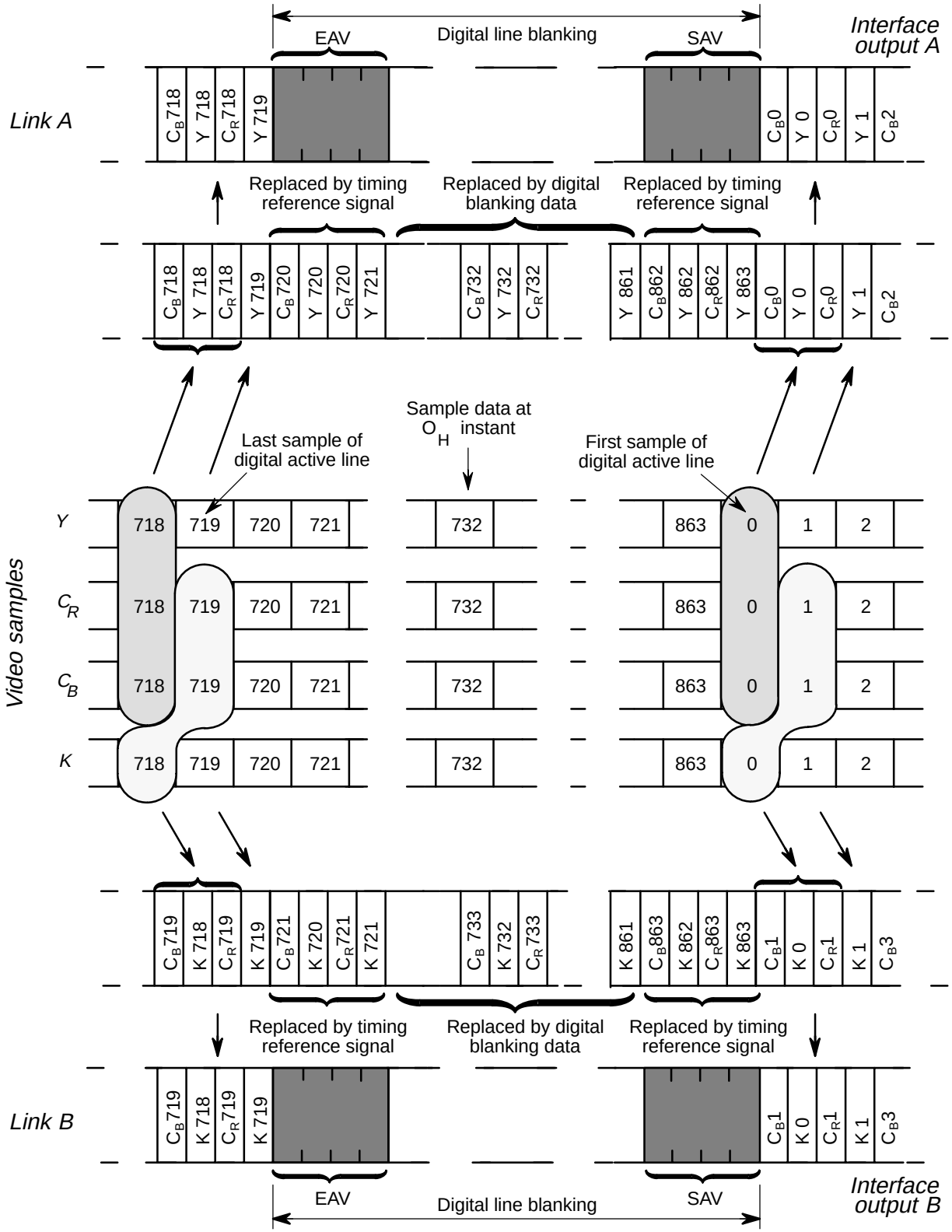


Fig. 4 – Composition of the data multiplex and position of the timing reference signals, EAV and SAV. (shown here for Link A carrying Y, C_R, C_B and Link B carrying K, C_R, C_B, sending end)

Table 3 – Protection bits in the timing reference signal.

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

5. Ancillary data signals

The ancillary data structure is to be defined fully in a separate document.

Unless it is the intended function of a particular item of equipment, the ancillary signals must not be modified by that equipment.

Ancillary data signals may be conveyed in 10–bit form during the line–blanking period only, and in 8–bit form only during the active line periods of lines in the field–blanking. (It should be noted that digital video tape recorders operating in accordance with CCIR Recommendation 657 do not record data in the line–blanking period, nor during some lines in the field–blanking period.)

The active portions of lines 20 and 333 are reserved for equipment and self–checking purposes.

The reserved data values $00.x_h$ and $FF.x_h$ (see *Section 2.2.*) are reserved for identification purposes and must not appear in the ancillary data.

All ancillary data signals carried during the active portions of lines in the field–blanking period must be preceded by the preamble:

00.x FF.x FF.x ZZ.x.

When ZZ has the value 15_h (8,4 Hamming–coded form of D9–D6 set to 0000), this indicates that there are no further ancillary data signals on that line. Any value of ZZ other than 15_h must be interpreted as indicating the presence of an ancillary signal immediately following the preamble.

The insertion of an ancillary data signal must result in the change of ZZ from 15_h, and must be accompanied by the insertion, immediately after the inserted data, of the preamble 00.x FF.x FF.x 15.x to indicate that the remainder of the line is available for the insertion of further ancillary signals.

6. Clock signal

The clock signal is sent on both Link A and Link B; it is at 27 MHz, there being 1728 clock intervals during each horizontal line period.

Chapter 2

Bit–parallel interface characteristics

1. Signal coding

1.1. Source signals

The bit–parallel interface carries data and clock signals as defined in *Chapter 1* of the present document.

1.2. Link–to–link timing relationship

The clock transitions for the two links shall lie within 10 ns of each other at the receiver[1].

2. Electrical characteristics

2.1. General

2.1.1. Hardware configuration

The parallel bit–streams (data plus clock) shall be transmitted via balanced signal pairs, respecting the polarity indicated in *Fig. 5*.

2.1.2. Time intervals

All time intervals specified in this *Chapter* are measured between the half–amplitude points of the signals.

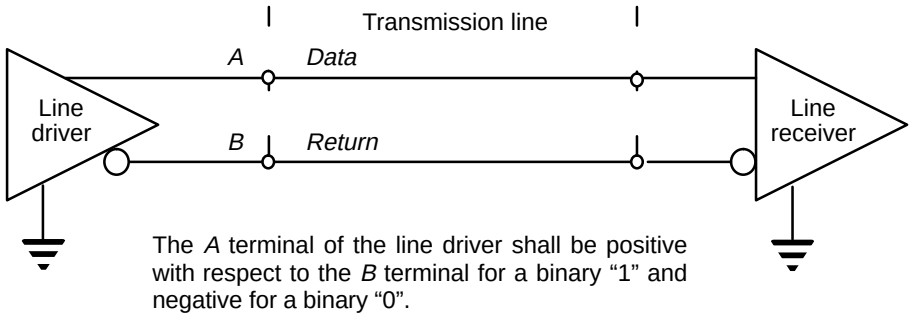


Fig. 5 – Convention defining the polarity of the binary signal.

1. Where the data receiver incorporates buffering to achieve synchronism between incoming data and an internal reference, or between sets of incoming data, this tolerance can be relaxed. However, it is anticipated that a common clock will be used in the sending equipment for both links, so that achieving this tolerance should present little difficulty.

2.1.3. Technology

Although the use of ECL technology is not specified, the line driver and receiver must be ECL–compatible i.e. they must permit the use of standard ECL components for either or both ends of the link.

2.2. Line driver characteristics

2.2.1. Output impedance

The line driver shall have a balanced output with maximum internal impedance of 110 ohms (as seen from the terminals to which the line is connected).

2.2.2. Common–mode voltage

The average voltage of both terminals of the line driver shall be –1.29 V ± 15% with reference to the ground terminal.

2.2.3. Signal amplitude

The signal amplitude shall lie between 0.8 V and 2.0 Vp–p measured across a 110–ohm resistor connected to the output terminals without any transmission line.

2.2.4. Rise and fall times

The rise and fall times, determined between the 20% and 80% amplitude points and measured across a 110–ohm resistor connected to the output terminals without a transmission line, shall be no longer than 5 ns and shall differ by not more than 2 ns.

2.3. Line receiver characteristics

2.3.1. Terminating impedance

The cable shall be terminated by 110 ohms ± 10 ohms.

2.3.2. Maximum signal input

The line receiver must correctly sense the binary data when connected directly to a line driver operating at the extreme voltage limits permited by *Section 2.2.3.*

2.3.3. Minimum input signal

The line receiver must correctly sense the binary data when a random data signal produces the conditions represented by the eye diagram in *Fig. 6* at the data–detection point.

Optionally, the line receiver may incorporate equalization and amplification circuits to permit correct operation with longer links. The line receiver must satisfy the maximum input signal conditions of *Section 2.2.3.*

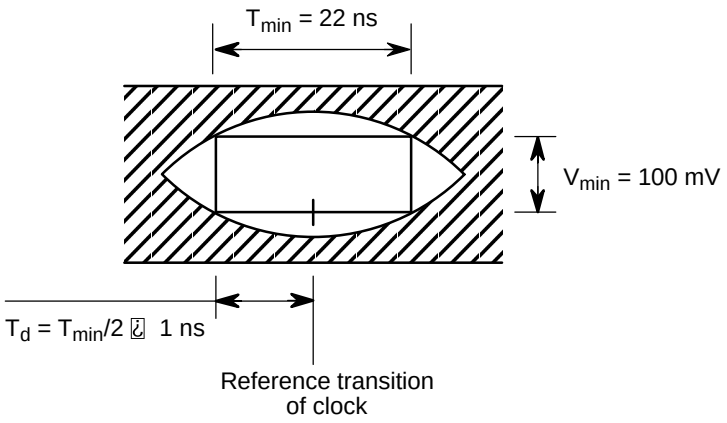


Fig. 6 – Eye diagram corresponding to the minimum input signal level.

2.3.4. Common–mode rejection

The line receiver must correctly sense the binary data in the presence of common–mode interference of ± 0.5 V, at frequencies in the range from 0 to 15 kHz.

2.3.5. Clock–to–data differential delay

The line receiver must correctly sense the binary data when the clock–to–data differential delay is ± 11 ns (see *Fig. 7*).

2.4. Clock signal

The specifications in this *Section* apply to the output of the line driver.

2.4.1. Clock pulse width

The clock pulse width is 18.5 ± 3 ns.

2.4.2. Clock jitter

The timing of individual rising edges of clock pulses shall be within ± 3 ns of the average timing of rising edges, as determined over at least one field.

2.4.3. Clock–to–data timing relationship

The positive transition of the clock signal shall occur midway between data transitions, as shown in *Fig. 7*.

3. Cables and connectors

3.1. Cable

3.1.1. Characteristic impedance

The cable used shall, for each data and clock pair, have a nominal characteristic impedance of 110 ohms.

3.1.2. Other characteristics

The differential delay introduced by the cable, between the clock and any data signal, shall not exceed 5 ns.

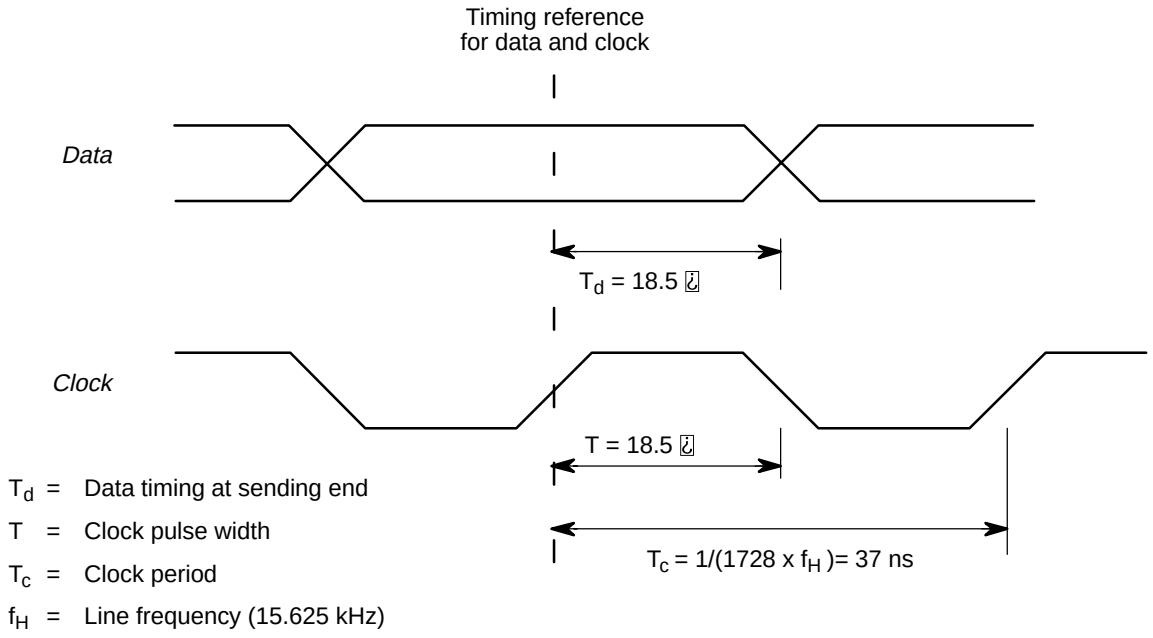


Fig. 7 – Clock–to–data timing relationship at the sending end.

It is strongly recommended that the cable should incorporate overall screening.

3.2. Connectors

3.2.1. Connector characteristics

The connectors shall have mechanical characteristics conforming to the standard 25–pin sub–miniature type D (ISO 2110–1980).

The cable assembly shall be provided at both ends with connector receptacles containing male contacts (plugs). Equipment inputs and outputs shall be equipped with connector receptacles containing female sockets.

Connectors are locked together with a screw lock, with a male screw on the cable connector and a female threaded post on the equipment connector. The threads are of type UNC 4–40. Details of the mounting post are shown in *Fig. 8*.

It is recommended that cable connectors should employ a conductive back shield to maintain screening of the signal conductors and care must be taken to select designs that are appropriate for use with the latching method specified.

3.2.2. Connector contact assignments

The contacts of the connector, numbered in the standard manner depicted in *Fig. 9*, are assigned in accordance with *Table 4*.

In order to achieve common numbering between 8–bit and 10–bit interfaces, *Table 4* shows assignments for 10–bit interfaces. For 8–bit interfaces, data bits D9 to D2 are used. The pair carrying the most–significant bit is assigned to contacts 3/16 in both cases, and no change is made to the assignments for 8–bit interfaces – only the signal name has been changed.

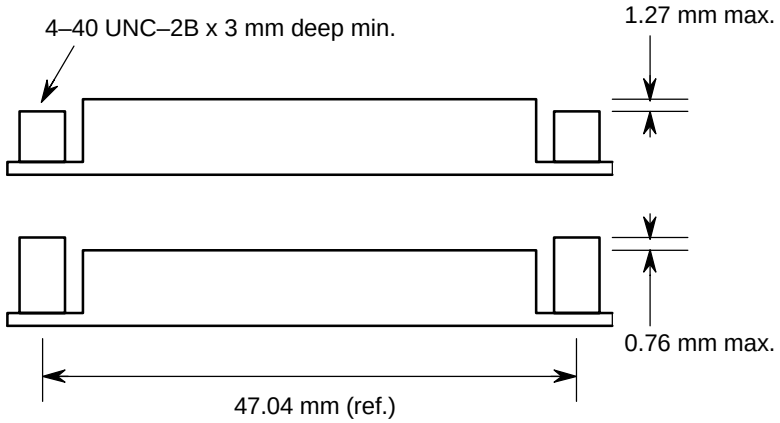
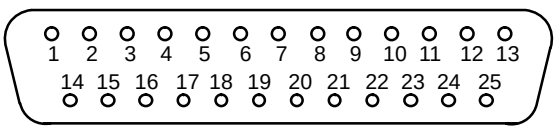


Fig. 8 – Detail of the DB25 connector mounting post.



Note: The preferred orientation for connectors, mounted vertically or horizontally, is with contact 1 uppermost.

Fig. 9 – Mating face of the connector receptacle containing male pins (plug).

Table 4 – Connector contact assignments.

Connector pin number	Signal line
1	Clock
2	System ground A
3	Data 9 (MSB)
4	Data 8
5	Data 7
6	Data 6
7	Data 5
8	Data 4
9	Data 3
10	Data 2
11	Data 1
12	Data 0
13	Cable shield
14	Clock return
15	System ground B
16	Data 9 return
17	Data 8 return
18	Data 7 return
19	Data 6 return
20	Data 5 return
21	Data 4 return
22	Data 3 return
23	Data 2 return
24	Data 1 return
25	Data 0 return

Note: The cable shield (contact 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that contact 13 should provide high–frequency continuity to the chassis ground at both ends and, in addition, provide DC continuity to the chassis ground at the sending end.

Chapter 3

Bit–serial interface characteristics

1. Signal coding

1.1. Source signals

The bit–serial interface carries data and clock signals as defined in *Chapter 1* of the present document.

1.2. Channel coding

The channel coding scheme shall be scrambled NRZI.

The generator polynomial for the scrambled NRZI sequence shall be G1(X).G2(X)

where: $G1(X) = x^9 + x^4 + 1$, to produce a scrambled NRZI signal

and $G2(X) = x + 1$, to produce the polarity–free NRZI sequence

The video data word size through the serial interface shall be 10 bits. The resulting nominal gross bit–rate is 270 Mbit/s.

1.3. Transmission order

The least–significant bit of any data word shall be transmitted first.

1.4. Differential timing

The interface must operate correctly when the electrical lengths of the interconnections between the line sender and the line receiver differ by up to 10 ns.

2. Electrical characteristics

2.1. Line driver characteristics

2.1.1. Output impedance

The line driver shall have an unbalanced output with a source impedance of 75 ohms and a return loss of at least 15 dB at frequencies in the range from 10 to 270 MHz.

2.1.2. Signal amplitude

The signal is conveyed in NRZI form using positive logic polarity. The peak–to–peak signal amplitude shall lie in the range 800 mV ± 10% measured across a 75–ohm resistor connected to the output terminals without any transmission line.

2.1.3. DC offset

The DC offset, as defined by the mid–amplitude point of the signal, shall lie in the range from + 0.5 to – 0.5 V.

2.1.4. Rise and fall times

The rise and fall times, determined between the 20% and 80% amplitude points and measured across a 75–ohm resistor connected to the output terminals without a transmission line, shall lie in the range from 0.75 to 1.50 ns, and shall not differ by more than 0.50 ns.

2.1.5. Jitter

The timing of the rising edges of the data signal shall be within ± 10% of the clock period, as determined over a period of one line.

2.2. Line receiver characteristics

2.2.1. Terminating impedance

The cable shall be terminated by 75 ohms, with a return loss of at least 15 dB at frequencies in the range from 10 to 270 MHz.

2.2.2. Receiver sensitivity

The line receiver must correctly sense random binary data either when connected directly to a line driver operating at the extreme voltage limits permitted by *Section 2.1.2.*, or when connected via a cable having a loss of 40 dB at 270 MHz and a loss characteristic of $1/\sqrt{f}$.

When receiving signals at levels between 0 and –12 dB with respect to the nominal level, no equalization adjustment shall be required. A requirement for adjustment is permitted at lower received signal levels.

2.2.3. Interference rejection

When connected directly to a line driver operating at the minimum level permitted in *Section 2.1.2.*, the line receiver must correctly sense the binary data in the presence of a superimposed interfering signal at the following levels:

DC:	± 2.5 V
below 1 kHz:	2.5 V_{p-p}
1 kHz to 5 MHz:	100 mV_{p-p}
above 5 MHz:	40 mV_{p-p}

2.2.4. Lock–up time

After a non–word–synchronous cut, the de–serializing operation shall achieve word synchronism in not more than one line–duration.

3. Cable and connector

3.1. Cable

3.1.1. Cable type

It is recommended that the cable should be chosen to meet any relevant national standards regarding electromagnetic radiation.

3.1.1. Characteristic impedance

The cable shall have a nominal characteristic impedance of 75 ohms.

3.2. Connector

The connector shall have mechanical characteristics conforming to the standard 75–ohm BNC type (IEC 169–8), and its electrical characteristics should permit it to be used at 500 MHz.

Appendix 1

Definitions

Binary	A number system with base 2.
Bit	An abbreviated form of the words “binary digit”; in binary notation, either “0” or “1”.
C_B	Colour-difference signal B – Y.
Clock signal	Timing pulses serving as a reference for a digital system.
C_R	Colour-difference signal R – Y.
Digital active line	The part of the television line period which conveys the digital video data words (C_B, Y, C_R, Y, etc.).
ECL	Emitter-coupled logic.
Electrical length	Physical length of a conductor, expressed in terms of propagation delay.
Hexadecimal	A number system with base 16 in which, in the written form, equivalents to the two-digit decimal numbers 10 to 15 are replaced by the letters A to F.
Interface	A concept involving the specification of the interconnection between two items of equipment or systems. The specification includes the type, quantity and function of the interconnection circuits and the type and form of the signals to be interchanged by these circuits. A *parallel* interface is one in which the bits of a data word are sent simultaneously on separate bearers. A *serial* interface is one in which the bits of a data word, and of successive data words, are sent consecutively on a single bearer.
Key signal	Signal derived from a video signal which actuates an electronic switch in the production of special effects.
LSB	Least-significant bit.
MSB	Most-significant bit.
Multiplex	The arrangement of the different component parts of the signal, for example Y, C_R, Y, C_B, so that the whole can be transmitted as a single data-stream.
NRZ	Non-return-to-zero.
NRZI	Non-return-to-zero with inversion.
Parity	A method by which binary numbers can be checked for errors. In a simple parity check, an extra bit called the parity bit, is added to make the sum of all the “1”s in the number consistently either odd or even (depending on whether odd or even parity is specified).
R, G, B	Red, green and blue primary signals.
Quantization	An operation which allocates to each sample a binary number of fixed length representing the amplitude of the sample with a degree of approximation which depends on the number of digits chosen.
Sample	The discrete instantaneous amplitude of a signal.
Word	A group or sequence of bits which are processed together.
Y	Luminance signal.

Appendix 2

Error detection and correction in the video timing reference signal

The following look–up table enables single–bit errors in the fourth word of the video timing reference signal to be corrected. Double errors, and some multiple–bit errors, are detected but not corrected. The code implemented for this purpose corresponds to an 8,4 Hamming code.

The table gives corrected values for F, V and H where possible. Multiple errors are indicated by asterisks.

Received P3–P0	Received F, V, H (bits 8 to 6)							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	110	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

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